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Novel Design and Simulation of HERIC Transformerless PV Inverter in MATLAB/Simulink

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Abstract—High conversion efficiency and improved safety standards are the key performance parameters analyzed by any photovoltaic (PV) inverter manufacturing company before embarking on full scale commercial production. Several inverter topologies have been proposed by different researchers in a bid to find a highly efficient topology that matches with the various grid codes. In recent years, the attention of the manufacturers has shifted to the transformerless PV inverters which have reduced weight, size and cost compared to the conventional inverter types. However, the substitution comes with new challenges of leakage current through the parasitic capacitance to the ground, which in turn affects it efficiency. Thus, many researches are ongoing to overcome these challenges while improving the inverters efficiency. The Highly Efficient and Reliable Inverter Concept (HERIC) is one of the proposed topologies. Therefore, this study focused on novel design and simulation of the HERIC transformerless PV inverter in MATLAB to determine its leakage current mitigation ability and improved performance efficiency. It was found out that, the topology is good in stabilizing the commonmode voltage of the highly fluctuations frequency, thus minimize the ground leakage current through the parasitic capacitance while at the same time keeping very high efficiency.

Keywords — HERIC; Leakage current; Common mode voltage; Efficiency; Transformerless PV Inverter.

I. INTRODUCTION

Solar photovoltaic (PV) panels used for electric power generation are not directly connected to the grid. This is because of differences in the type of power generated and the power required by both the solar panels and the grid; as such, dc (direct current)-to-ac (alternating current) inversion is required. In order to efficiently convert the energy produced and smooth grid connections, an efficient power electronics converter designs are necessary [1], [2]. Safety of operations, grid protection and increase reliability as well as efficiency optimization of the solar panels are achieved through accurate design of the DC-AC inverters [3], [4]. Nevertheless, ability to inject pure sinusoidal current in phase with the grid voltage into the grid has be to achieved.

Previously, power electronics converters are designed with small to large size transformers; which resulted to so many challenges of weight, cost, size and reduced efficiency [4]-[6]. With recent advances in technology, the design of transformerless PV inverters evolved in order to address the aforementioned challenges of the conventional design. However, leakage current and common mode voltage are part of the major technical challenges of the grid-connected transformerless PV inverters [4]-[6]. Leakage currents flowing through the parasitic capacitance of the photovoltaic array and the grid result in severe voltage lose.

Recently, different forms of single-phase transformerless PV inverter topologies were proposed with the aim of complying with various grid codes [4], [6]. The most popular among the proposed topologies include H5, H6, HERIC, REFU, FB-DCBP, FB-ZVR, NPC, Conergy NPC and so on. The aim is to suppress the main source of leakage current, i.e. the change in common mode voltage [6]. All new topologies are developed to achieve at least better performance than traditional full-bridge inverter (H4). In this study, MATLAB/Simulink was used to design and simulate the HERIC transformerless PV interver, while at the same time evaluating its performance in terms of efficiency, suppression of leakage current and electromagnetic interference (EMI). The schematic diagram of the HERIC inverter topology is shown in Fig. 1.



Fig. 1. Schematic diagram of HERIC inverter topology [5]

II. MATERIALS METHOD

A. Simulation Model Establishment

A new simulation file was created on the Simulink window, the circuit and device modules were extracted from the Library Browser. The circuit components were carefully connected in accordance with the procedure described in [5]. The main components of the circuit are DC source (PV panel), capacitor, switching devices (IGBTs), inductor, SPWM generator etc. Similarly, unipolar sine pulse width modulation (SPWM) signal source was used to trigger the IGBTs. The triggering pulse (SPWM) was connected to the gate of the corresponding IGBTs. The waveforms of the sinusoidal output voltage (V_AC) and current (I_AC) across the load, leakage current, common mode voltage, efficiency and other performance parameters were observed and recorded. The control and power stages of the proposed inverter topology are shown in figures 2 & 3 respectively.



Fig. 2. Control stage of the HERIC inverter



Fig. 3. Power stage of the HERIC inverter

B. Setting of Simulation Parameters

Parameters used during the model establishment are shown in the Table I. The IGBTs parameters were set to default values, while the phase delay of the pulse generators was set at corresponding static values. The simulation termination time of 0.1s was used throughout.

TABLE I.	SIMULATION	PARAMETERS

Parameter	Value			
Input DC link voltage: V_{dc}	290V			
Series RLC resistor: R_{dc}	1x10 ⁻⁵ ohms			
Input DC link capacitance: C_{dc}	0.94F			
Grid load: Grid _{load}	10.68 ohms			
Maximum output power: Po	1000 W			
Output filter $L_1 = L_2$	0.01 H			
Switching frequency: f_S	16 k Hz			

C. Simulation Control and Operations

The parameters control and operations for the conduction states of the HERIC topology used in the study is similar to the one proposed by Chu and Hamid et. al [7], [8] as shown in Table II.

S1	S2	S 3	S4	S5	S 6	No of conducting switches	V_{AB}	I _{grid}
ON	OFF	OFF	ON	OFF	ON	2	>0	>0
OFF	OFF	OFF	OFF	OFF	ON	1	0	>0
OFF	ON	ON	OFF	ON	OFF	2	<0	<0
OFF	OFF	OFF	OFF	ON	OFF	1	<0	<0

TABLE II. CONDUCTION STATES OF HERIC TOPOLOGY [9]

The control signals of the topology is shown in Fig. 4. The HERIC topology has four modes of operation. In the first mode, the switches that conduct are S1& S4. In the second mode, the switches that conduct are S5& S6. Whereas, in the third mode, the conducting switches are S2 & S3. Finally, S5 & S6 switches conduct in the fourth mode.



III. SIMULATION RESULTS AND WAVEFORM ANALYSES

A. Load Output Voltage (V AC)

Figure 5 shows the load side output voltage (V_AC). It can be seen from the figure that the waveform is close to pure sinusoidal as expected in the ideal condition [4]. However, in the absence of LCL filter, the expected shape will not be obtained. Similarly, power losses of the switching devices also contributed towards that.



Fig. 5. Load output voltage

B. Load Current (IL)

Figure 6 shows the load current (I_L) . It can be seen from the figure that the waveform is close to pure sinusoidal as expected in the ideal condition. Similar explanations hold as that of the load voltage.



Fig. 6. Load current

C. Leakage current (I_{Cpv}) and common-mode voltage (V_{Cpv})

Figure 7 shows the leakage current and the common-mode voltage obtained. It can be seen from the figure that, the high frequency fluctuations of the common-mode voltage due to unstable voltage supply of the PV panel is drastically minimized or almost made constant. As a result, the leakage current is significantly reduced, thereby increasing the inverter efficiency.



Fig. 7. Leakage current (I_{Cpv}) and common-mode voltage (V_{Cpv})

IV. CONCLUSIONS

Three level output voltage was achieved in the proposed HERIC inverter topology using the same frequency as the switching one. The common-mode voltage fluctuations were also minimized, thus, significantly reduces the leakage current through the parasitic capacitance. These keep the efficiency of the HERIC topology higher than the full-bridge inverter topology.

A. Precautions

- 1. IGBT was used as the switching device throughout the simulation.
- 2. Sine pulse width modulation (SPWM) signal source was used in firing the IGBTs throughout the simulation.
- 3. The DC voltage source and the load were connected to the *common ground* to minimize voltage losses and avoiding short circuit fault when implementing the prototype.

B. Suggestions for Future Studies

Validation of the proposed inveter topology via prototype development is beyond the scope of this research study. It is suggested that this should be part of a future study's objectives.

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CONFLICTS OF INTEREST

The authors declare that they have no conflicts of interest.

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