Analysis of Three Phase Quasi Switched Boost Inverter Topology for Renewable Energy Applications

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Abstract- *A class of single phase quasi Switched Boost Inverter (qSBI) topology is developed for low power Renewable Energy Source (RES) applications. This paper analyzes a three phase Embedded type qSBI (E-qSBI) topology which is capable of boosting and inverting the available dc voltage in a single stage. The operating modes, steady state analysis and PWM (Pulse Width Modulation) control of the boost inverter topology is discussed in detail in this work. The E-qSBI supplying, 100W RL-Load is designed and simulated with MATLAB/Simulink software tool. The Fast Fourier Transform analysis (FFT) of output voltage waveform is carried out and the harmonic profile is presented. The simulation results are presented to show the effectiveness of single stage embedded type qSBI topology.*

Keywords- Switched Boost Inverter (SBI), Embedded type quasi Switched Boost Inverter (E-qSBI), simple boost control, shoot-through, Z Source Inverter (ZSI)

1. INTRODUCTION

Renewable energy is considered highly essential for meeting present and future energy demands. Solar photo voltaic is probably the best technology among all energy sources because of its clean and unlimited source of energy [1]. The Voltage Source Inverter (VSI) performs as a power electronic interface between RES and the grid [2, 3]. It is essential to connect a classical boost converter in cascade with the VSI to avail the boosted ac voltage when the available dc source voltage is insufficient. So the resulting power converter structure becomes bulky and costly. In conventional VSI, both the upper and lower power devices in a single leg should not be on simultaneously since it causes short circuit in power supply. Dead time, shoot through and Electro Magnetic Interference (EMI) are the major issues in traditional VSI.

To overcome all the above mentioned issues, Z Source Inverter (ZSI) are proposed in 2002 [4-6], which can perform both, boosting and inversion action in a single stage using shoot-through. ZSI uses a lattice network, consists of two symmetrical LC components to boost the available voltage. Modified topologies of ZSI like, quasi ZSI (q-ZSI), extended boost ZSI/ q-ZSI [7], are presented to obtain continuous input current. In case of Trans Z Source Inverter (Trans ZSI), high boosted voltage can be obtained with the help of a transformer with less number of capacitors [8]. In traditional ZSI, inductors are used to attain high voltage gain whereas switched inductor cells are used in switched inductor ZSI [9]. The tapped inductor ZSI (TL-ZSI [10]) and TZ-Source Inverter (TZSI) possess all the advantages of traditional ZSI by using transformer. There are cascaded TZSIs, cascaded multi cell Trans ZSIs, alternate cascaded switched/ tapped inductor cells are available in literature [11-14]. But the practical implementation of symmetrical impedance network in ZSI is not possible. Due to the asymmetrical network, ZSI has high magnetic requirements and poor transient response [15, 16]. All the above mentioned ZSI topologies are of bulky in size, heavy and of large volume. The large value of passive components causes high loss and reduced efficiency. So ZSI may not be best suited for Nano grid connected photovoltaic applications.

To eliminate the complexities addressed under ZSI and its modified topologies, Switched Boost Inverters (SBI) are proposed in [15-18]. The SBI is basically derived from Watkins-Johnson topology. The SBI inherits all the properties of ZSI. The SBI has reduced passive components count and an additional power device compared to ZSI. Also SBI can provide ac and dc voltages simultaneously. But its input current is discontinuous.

To eliminate the drawbacks of SBI, Current Fed Switched Inverter (CFSI) is suggested in [19]. The CFSI has the boost factor (1-D) times more than that of SBI. To produce high voltage gain, CFSI needs to be operated at high shoot through duty ratio which makes modulation index very less. Due to the decrement in modulation index, the Total Harmonic Distortion (THD) in the load voltage and load current is increased and the overall gain is reduced. A family of single phase quasi Switched Boost Inverter (qSBI) is proposed in [20]. There are basic qSBI, embedded qSBI, dc linked qSBI discussed in [20].

In this study, a three phase Embedded type qSBI (E-qSBI) is designed to feed 100W RL load. The modified Simple Boost PWM control technique is adopted to analyze the modes of operation. The MATLAB /Simulink tool is used for analyzing the topology and the simulation results are presented. With the input voltage of 32V and output ac peak voltage of 150.36V, the gain of 4.6 is obtained. The performance comparison between three phase basic SBI and three phase embedded type qSBI is discussed. The harmonic content in the output voltage is analyzed and presented.

2. CONVENTIONAL ZSI, SBI, E-QSBI TOPOLOGIES

Fig.1 shows the conventional ZSI topology proposed in [4]. It consists of a diode, a LC network and an inverter bridge. Fig.2 shows the conventional SBI topology proposed in [15]. In basic SBI, both the source and inverter bridge are sharing the common ground. It consists of a pair of diode (D_1, D_2), single inductor and capacitor (L, C), a single power switch(S) and an inverter bridge. The expression for boost factor in conventional ZSI and SBI is derived as [4],

$$B = \frac{1-D}{1-2D} \tag{1}$$

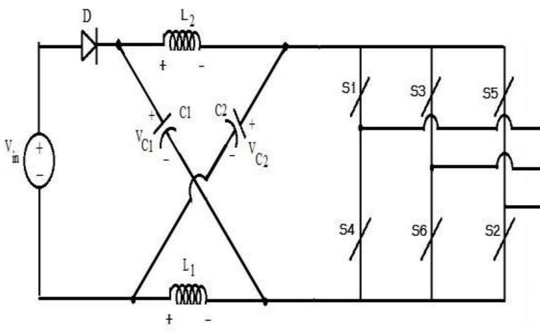


Fig.1 Z-Source Inverter Topology

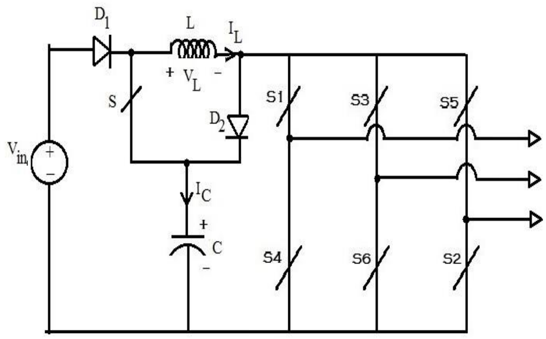


Fig.2 Switched Boost Inverter (SBI) Topology

3. THREE PHASE EMBEDDED TYPE QSBI OPERATING CONDITION

Fig.3 shows the circuit diagram of E- qSBI. It consists of a single inductor L and a capacitor C, eight diodes, seven power devices and a RL load (R_l and L_l). Fig.4 (a) shows the shoot through state during which the inverter leg is shorted by turning ON both the upper and lower switches. The time interval of shoot through state is $D \cdot T_S$ where D is the duty ratio and T_S is the switching time period. During this period, the switch S is on: and D_1, D_2 are reverse biased. The capacitor C charges the inductor. The voltage across the inverter bridge is zero. There is no power flow across the load.

The non-shoot through state is shown in Fig.4 (b). During this state, the inverter has six active states and two open states. The time duration for this mode is $(1-D) \cdot T_S$ and during this state D_1, D_2 are forward biased and active switch S is kept off. The inductor transfers energy to the inverter circuit while the capacitor is getting charged. During this interval, the capacitor voltage is equal to the voltage across the inverter bridge. During shoot through state, the voltage across the inductor and the current through the capacitor are given by,

$$V_L = V_{in} + V_C \ , \tag{2}$$

$$I_C = -I_L \, .\tag{3}$$

where V_L is voltage across the inductor; V_{in} is the input voltage; V_C is the voltage across the capacitor, I_C Is the current through the capacitor, I_L is the current through the inductor.

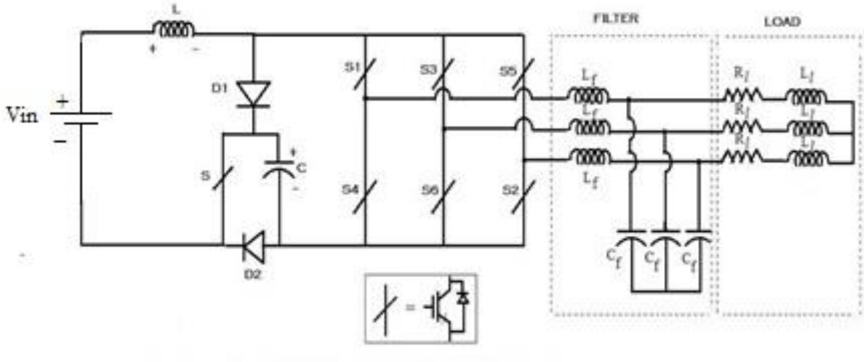


Fig. 3 Three Phase Embedded type q-SBI supplying RL-Load.

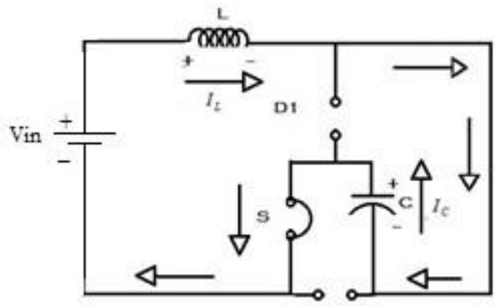


Fig.4 (a) Shoot through

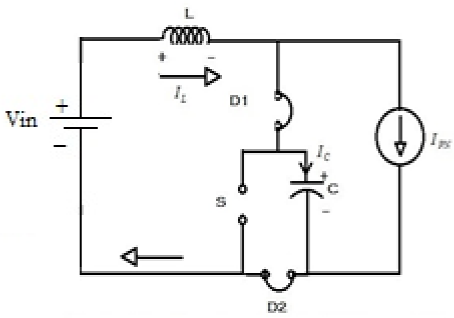


Fig.4 (b) Non-shoot through mode of E-qSBI

During non-shoot through state, the inductor voltage and capacitor current are given by,

$$V_L = V_{in} - V_C \, ,\tag{4}$$

$$I_C = I_L - I_{PN} \, .\tag{5}$$

where, I_{PN} is the inverter bridge current.

After applying volt second balance to the voltage across the inductor,

$$D(V_{in} + V_C) + (1 - D)(V_{in} - V_c) = 0\tag{6}$$

After applying charge second balance to the current through the capacitor,

$$D(-I_L) + (1 - D)(I_L - I_{PN}) = 0\tag{7}$$

The expression for voltage across the capacitor is given by,

$$V_C = \frac{1}{1 - 2D} \cdot V_{in}\tag{8}$$

The expression for current through the dc link is given by,

$$I_{PN} = \frac{1-2D}{1-D} \cdot I_L \tag{9}$$

The peak DC link voltage that appears across the inverter circuit is given by,

$$V_{PN} = V_C = \frac{1}{1-2D} \cdot V_{in} \tag{10}$$

The boost factor (B) is expressed by

$$B = \frac{V_{out}}{V_{in}} = \frac{1}{1-2D} \tag{11}$$

4. The PWM strategy of three phase embedded type qSBI [25]

Fig.5 shows the simple boost modulation technique of three phase E- qSBI [25]. The shoot through state of the inverter bridge is required to obtain higher boost in the embedded type qSBI. For that the additional active switch S needs to be operated along with the power switch in the inverter bridge. The conventional sinusoidal PWM technique cannot be applied to generate gate signals of three phase E type-qSBI. There are three modulation signals $V_{ma}, V_{mb,} V_{mc}$. The pulses for the switching devices in the inverter bridge circuit are produced by comparing these three sinusoidal signals and triangular carrier signal (V_{tri}) with high frequency. The positive and negative shoot through envelopes $+V_{st}$ and $-V_{st}$ are compared with the triangular pulse V_{tri} to produce gate signals for switch S. The gate control signals at ωt = 0 is shown in Fig.5

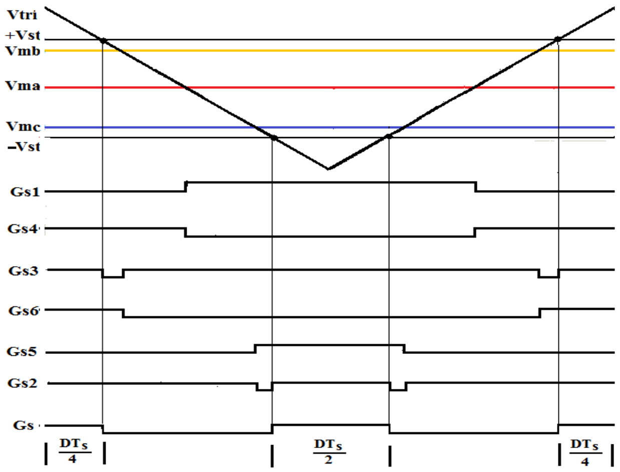


Fig.5 Simple Boost PWM control of Three Phase E-qSBI

The fundamental peak ac load voltage is given by,

$$\hat{V}_{ac} = M \cdot \frac{1}{1-2D} \cdot V_{in} \tag{12}$$

The voltage gain is expressed as,

$$G = \frac{M}{(2 \cdot M) - 1} \tag{13}$$

In the modified simple boost PWM control, the sum of M and D should not exceed the value of unity so that the shoot through gating pulses can be accommodated into the conventional zero states. The above discussed PWM Control strategy can provide only the open loop control of E-qSBI. The closed loop control technique explained in [18] is applicable to E-qSBI also.

5. DESIGN OF PASSIVE COMPONENTS

The inductance and capacitance values are calculated by considering the inductor ripple current and capacitor ripple voltage as,

$$\Delta I_L = \frac{V_{in} + V_C}{L} \cdot D \cdot T_S, \tag{14}$$

$$\Delta V_C = \frac{I_L}{C} \cdot D \cdot T_S. \tag{15}$$

The filter inductor L_f and capacitor C_f are designed at fundamental frequency of 50Hz with unity gain [19].

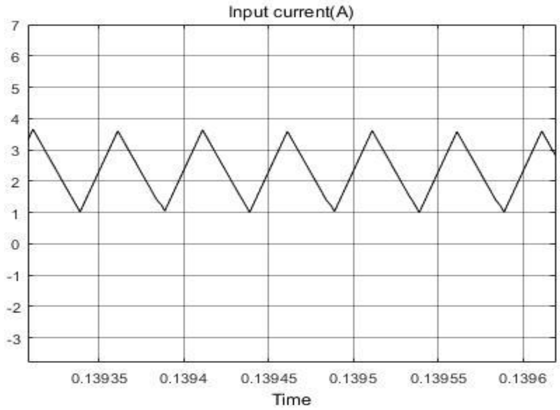
6. SIMULATION RESULTS

To analyze the performance of three phase E-qSBI simulations are done with MATLAB / Simulink. The simulated output voltage, load current, DC link boosted voltage, capacitor voltage, input current are presented with RL load. The dc voltage of 32V is boosted and inverted with the modulation index of M = 0.5, shoot through duty ratio of D =0.453 and switching frequency of f_S = 10 kHz for all power switches.Table.1 presents the design parameters of three phase E- qSBI.

Table 1 Design Specifications

Parameters	Values
Supply Voltage	32V
RMS Output Voltage	110V
Capacitor	470μF
Inductor	3mH
Filter Capacitor	10μF
Filter Inductor	3mH
RL load	R_l = 100 Ω, L_l = 5 mH.

The input voltage and current waveforms of three phase embedded type qSBI are given in Fig.6. The voltage stress across the switch S is presented in Fig.7. The entire dc link voltage of about 282V appears as the voltage stress across the switch.



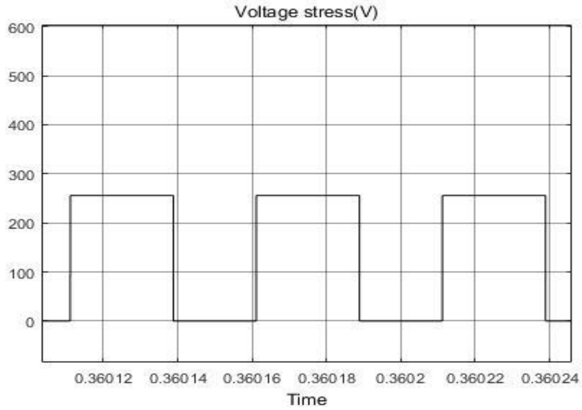
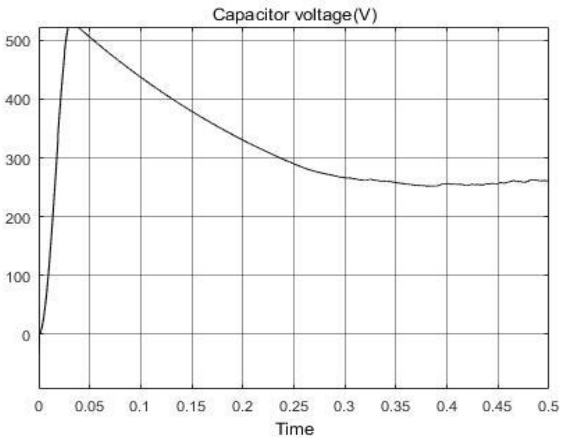


Fig.6 Input voltage and input current waveform of

Fig.7 Voltage Stress across switch S

Three Phase E-qSBI

The voltage across the capacitor and current through the inductor are presented in Fig.8(a) and Fig.8(b).



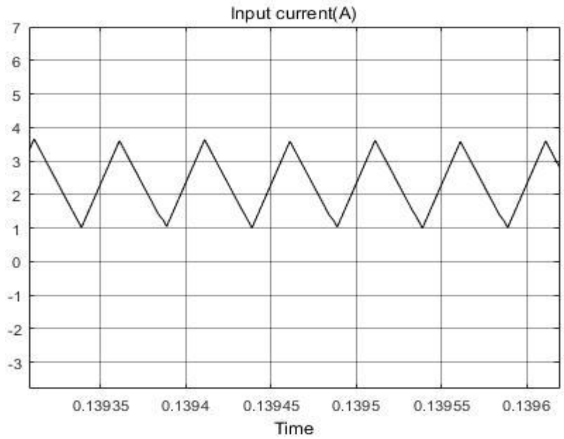


Fig.8 (a) Capacitor Voltage (V)

Fig.8 (b) Inductor Current (A) Waveforms

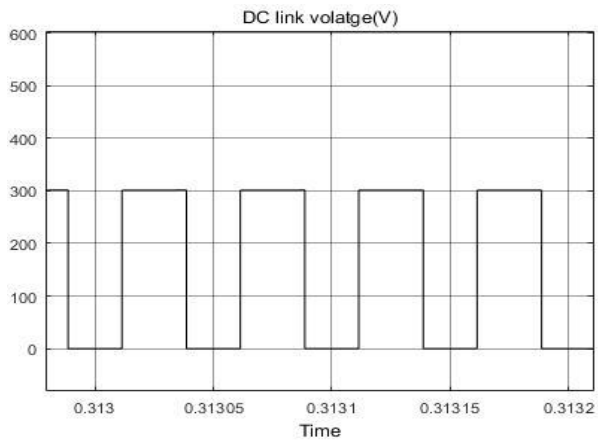
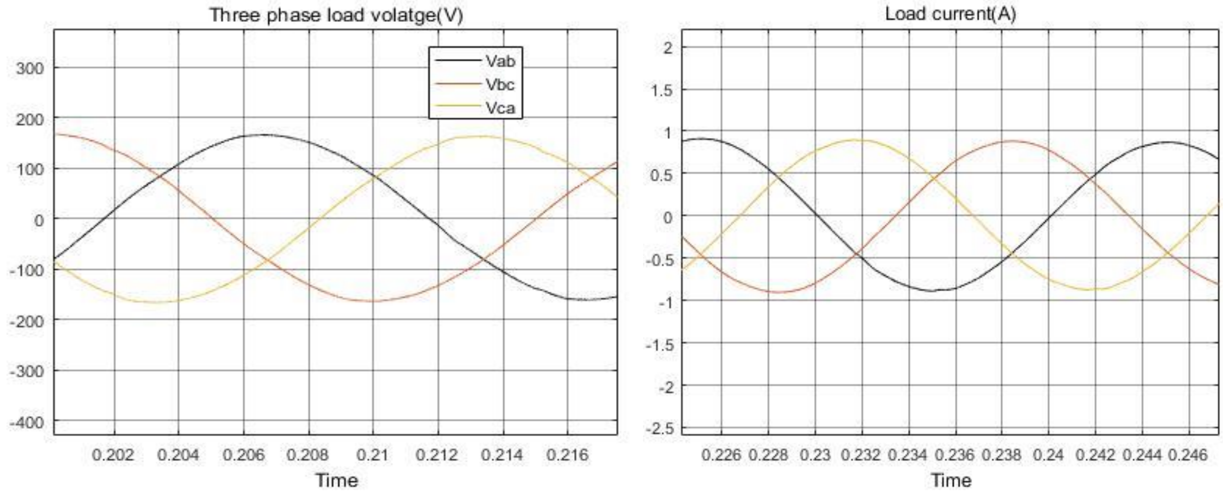


Fig.9 DC Link Voltage across Inverter Bridge

Fig.9 presents the dc link voltage across the inverter bridge. Fig.10 (a) and Fig.10 (b) shows the three phase filtered load voltage and load current waveforms across the load terminals. It is understood that the input of 32V provides the filtered ac peak output voltage of 150.36V (rms voltage of 106.32V) and the peak load current of 0.75A. The converter provides the output power of 97.5W and gives the efficiency of 97.5% for the specification given in Table 1. Due to snubber resistances and capacitances in switching devices, there are power losses which reduced the designed output load voltage.



(a) **(b)**

Fig.10 Three phase Output Voltage and Current Waveforms across Load Terminals

7. PERFORMANCE EVALUATION OF THREE PHASE EMBEDDED TYPE QSBI WITH CLASSICAL ZSI AND SBI

The output RMS voltage of conventional VSI, SBI, and Embedded type qSBI with V_{in} = 32V, M=0.5, D=0.453 are obtained as follows [26]:-

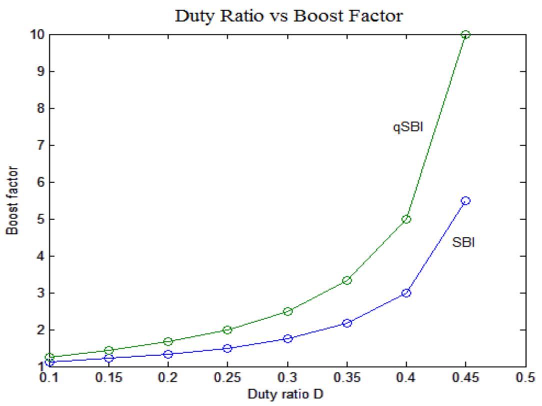
RMS line voltage of classical VSI = $\frac{\sqrt{3}\cdot M\cdot V_{in}}{2\cdot\sqrt{2}} = 10.77V$ (16)

RMS line voltage of traditional SBI= $\frac{\sqrt{3}\cdot M\cdot V_{in}}{2\cdot\sqrt{2}}\cdot\frac{1-D}{1-2D} = 57.205V$ (17)

RMS line voltage of embedded type qSBI= $\frac{\sqrt{3}\cdot M\cdot V_{in}}{2\cdot\sqrt{2}}\cdot\frac{1}{1-2D} = 106.32V.$ (18)

From the above expressions, it can be concluded that for same supply voltage and modulation index, the three phase embedded type qSBI can provide higher ac output voltage. If a dc load is connected in parallel to the capacitor, dc power could be supplied to the load. Thus, this topology can produce both dc and ac voltage as well.

The Fig.11 shows the comparison between boost factor and duty ratio of three phase SBI and three phase embedded type qSBI.



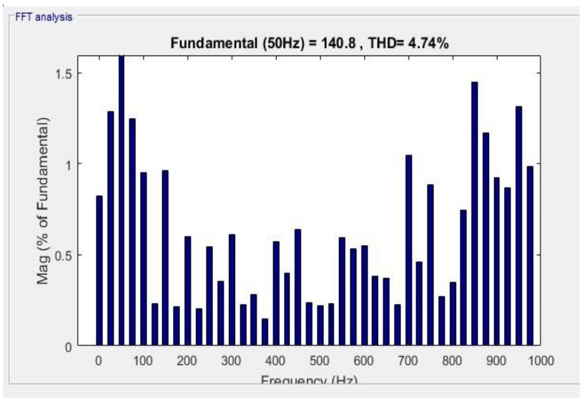


Fig.11 Comparison between Boost Factor and Duty Ratio **Fig.12** Harmonic profile of load voltage of E-qSBI

The Fig.12 shows the harmonic profile of load voltage of E-qSBI. It is explicit that the Total Harmonic Distortion (THD) of E-qSBI for the above mentioned design specifications are 4.74% which meets the IEEE standard.

8. CONCLUSION

The working principle and steady state analysis of three phase embedded type quasi Switched Boost Inverter (E-qSBI) is explained in detail. The implementation of PWM control of embedded type qSBI is also elaborated in this paper. The measured efficiency of the three phase E-qSBI is 97.5% with the duty ratio of D=0.453 and the output power of 97.5W. The harmonic profile of filtered load voltage is negligible due to the absence of dead time. The simulation results obtained are very well in consistent with theoretical expressions and it can be concluded that E-qSBI is best suited for renewable sources based high voltage gain applications. The results can further be verified with the hardware implementation. This work can be extended to detain the dynamic stability by implementing a suitable closed loop control technique.

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