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# Design and Implementation of Feedback Controller for Non-Isolated Switching DC-DC Buck Converter Operating in Continuous Current Conduction Mode

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**Abstract.** DC-DC converters are one of the major research areas in the field of power electronics. Design oriented study of lead compensator as well as Type-3 compensator is carried out and compared for its effectiveness in control of DC-DC Buck converter. Design and development of lab prototype of 5 V, 3 A voltage regulated Buck converter operating at switching frequency of 25 kHz is carried out involving design and fabrication of power circuit, MOSFET gate-driver circuit and controller circuit. The control circuit is implemented using PWM controller IC SG3525AN. The bode diagrams of control to output transfer function, uncompensated as well as compensated loop gain are plotted and verified to achieve required gain crossover frequency and phase margin with high loop gain at low frequencies leading to zero steady state error. Developed lab prototype of the Buck converter thoroughly tested on resistive load and experimentally verified for its dynamic performance as well as stable close loop operation.

**Keywords:** Buck Converter, Point of Load Converter, Lead Compensator, Type-3 Compensator, Gain Crossover Frequency, Control to Output Transfer Function, Uncompensated system, Compensated system, Loop gain, Steady state error.

## 1 Introduction

Buck converter is non-isolated type of switching DC-DC converter [1], [2]. It is the most common and simplest converter. It is also known as step down converter as the output voltage (V) is always less than the input voltage ($V_g$). Polarity of the output voltage is same as that of the input voltage. Fig. 1 shows the basic circuit diagram of Buck converter. Switch Q is semiconductor switch. D is the free-wheeling diode. Switch Q is repeatedly made on and off. This switching action causes a train of pulses which is filtered by second order low-pass filter formed by inductor, L and capacitor, C to generate low ripple DC output voltage (V).

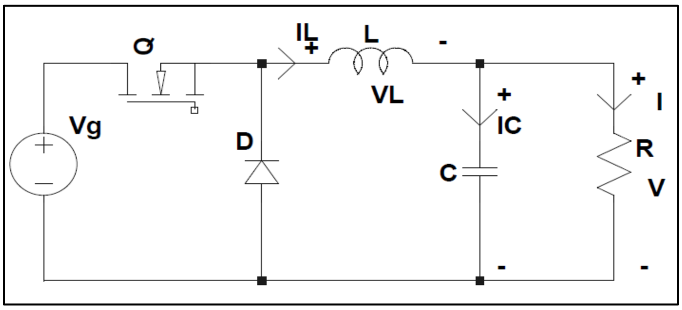


**Fig. 1.** Circuit diagram of Buck converter.

Buck Converter as well as other non-isolated DC-DC switching converters are widely used as point-of-load (POL) power supply to provide well-regulated low value DC output voltage to variety of electronic loads from an intermediate DC input voltage bus or from battery voltage in battery powered appliances such as mobile phones, laptop computers etc. where precise regulation of output voltage and fast dynamic response are major requirements apart from high-efficiency and small size [3]. Voltage mode control and current mode control are the commonly used PWM control techniques for control of DC-DC switching converters [2], [3]. Voltage mode control of the Buck converter with proportional controller is described in reference [4]. Compensator design procedure for Buck converter with voltage-mode error amplifier is given in reference [5]. This paper reports design oriented study, implementation as well as experimental testing and validation of voltage mode controlled Buck converter operating in continuous current conduction mode (CCM) with Type-3 compensator. Section-2 of the paper discusses modelling as well as compensator aspect related to close loop control of DC-DC converter. Section-3 describes design, implementation and development of lab prototype of voltage mode controlled Buck converter and presents experimental results obtained during testing of the converter verifying the design.

## 2 Closed Loop Control of DC-DC Converter

Block diagram for closed loop voltage mode control of Buck converter is shown in Fig. 2 [2]. In voltage regulated Buck converter, output voltage, v(t) is required to be maintained constant against disturbances in input voltage, $v_g(t)$ and load current $i_{load}(t)$ as well as changes in circuit parameters. To achieve this, we introduce a compensator in the forward path whose main function is to adjust duty cycle, d(t) in such a way that desired output voltage is maintained regardless of line and load disturbances. For proper and stable close loop operation, the compensator is to be designed in such a way that, it provides high gain at low frequencies, low gain at high frequencies and adequate phase margin between 45˚ to 80˚ with required gain cross-over frequency.

Let, $G_{vd}(s)$: Control to output transfer function

$G_{vg}(s)$: Line to output transfer function

$Z_{out}(s)$: Output impedance
T(s): Open loop transfer function or loop gain
$G_c(s)$: Transfer function of the compensator
$G_{PWM}(s)$: Transfer function of the PWM comparator
H(s): Transfer function of sensor

Loop gain is given by,

$$T(s) = G_c(s)G_{PWM}(s)G_{vd}(s)H(s)$$

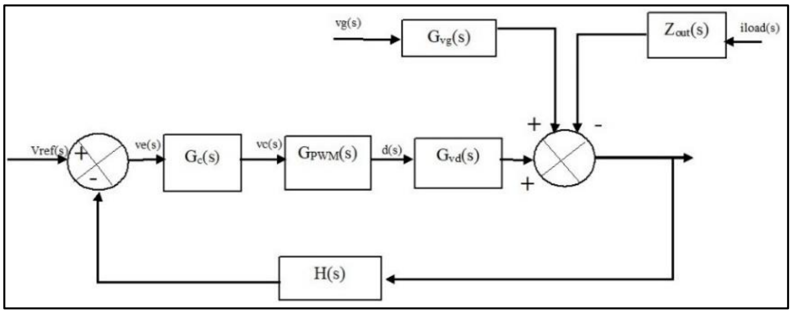


**Fig. 2.** Block diagram of Buck converter operating in closed loop voltage mode control

### 2.1 Lead Compensator

Lead compensator is used to improve the phase margin of the system [2]. Transfer function of the Lead compensator is,

$$G_c(s) = G_{co}\ (1 + s/\omega_z)/(1 + s/\omega_p)$$

A zero is added to the loop gain, at a frequency $f_z$, sufficiently far below the crossover frequency, $f_c$ such that the phase margin of the loop gain T(s) is increased by the required amount. Compensator also adds pole at high frequency which has beneficial effect of attenuating switching frequency noise. Disadvantage of lead compensator is that it gives low gain at low frequency which gives non-zero steady-state error in the converter output voltage. Therefore, the controller should be of Type-3 controller which has three poles and two zeros including one pole at origin.

### 2.2 Type-3 Compensator

Type-3 compensator provides three poles and two zeros including one pole at origin [5], [6]. Transfer function of Type 3 compensator is,

$$G_c(s) = (G_{co}(1+s/\omega_z)(1+s/\omega_{z1}))/(s/\omega_{z1}(1+s/\omega_p)(1+s/\omega_{hp}))$$

It is modified version of Lead compensator with one additional pole at origin ($f_{po}$), one additional zero ($f_{z1}$) sufficiently below crossover frequency ($f_c$) and one more additional pole ($f_{hp}$) sufficiently far away from crossover frequency ($f_c$). It is used when more than 90 degrees of phase boost are necessary with high gain at low frequency.

# 3 Lab Prototype and Experimental Results

In this section, design and implementation aspects of lab prototype of 5 V, 3 A close loop voltage mode controlled voltage regulated Buck converter operating at switching frequency of 25 kHz are described and obtained experimental results while testing the developed converter are presented as well as discussed.

## 3.1 Buck Converter Design Specifications

A Buck converter and its compensator are designed and developed to comply with specifications as given in Table 1

**Table 1.** Design specifications

| S. No. | Specification/ Parameter | Value |
|---|---|---|
| 1. | Input voltage ($V_g$) | 15 V |
| 2. | Switching frequency ($f_s$) | 25 kHz |
| 3. | Load resistance (R) | 1.667 Ω |
| 4 | Peak to peak value of saw-tooth waveform ($V_m$) | 2.4 V |
| 5 | Output voltage (V) | 5 V |
| 6 | Filter inductor (L) | 150µH |
| 7 | Output voltage ripple (ΔV) | ≤ 50mV |
| 8 | Reference voltage ($V_{ref}$) | 5 V |
| 9 | Filter capacitor (C) | 220 µF |
| 10 | Crossover frequency ($f_c = f_s/10$) | 2.5 kHz |
| 11 | Phase margin (PM) | 60˚ |
| 12 | Steady state error | 0 |

**Design Calculations:**

For the CCM Buck Converter,

Duty cycle, D = ($V/V_g$) = (5/15) = 33.33%, Load current, I = (V/R) = (5/1.667) = 3 A.

Here H is DC gain of the output voltage sensor, which is given by

$$1/H = V/ V_{ref,}$$

Hence, H = 1. Transfer function of the PWM comparator is given by,

$$G_{PWM}(s)=1/V_m$$

Control to Output transfer function for Buck converter operating in CCM [2],

$$G_{vd}(s)=V_g/(1+Ls/R+s^2LC)$$

For our designed Buck converter, control to output transfer function is given by,

$$G_{vd}(s) = 15/(1+150\times10^{-6}s/1.667+s^2(150\times10^{-6}\times220\times10^{-6})) \qquad (1)$$

Fig. 3 shows bode plot of control to output transfer function.

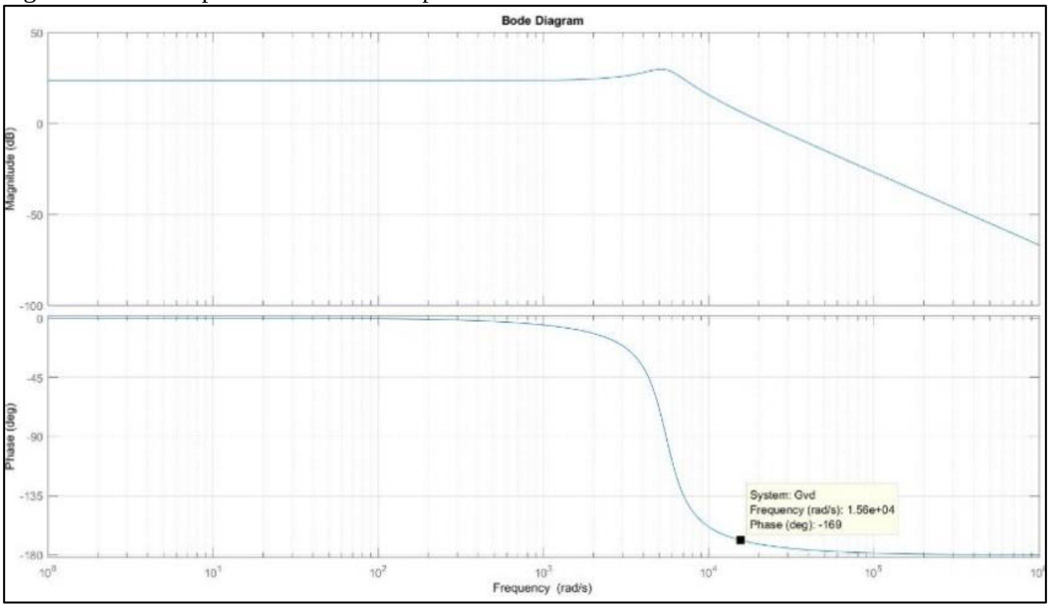


**Fig. 3.** Bode plot of control to output Transfer function

Normalized form of control to output transfer functions is,

$$G_{vd}(s) = 15/(1+s/Q\omega_o+s^2/\omega_o^2) \qquad (2)$$

Comparing equations (1) and (2) gives,
Quality factor, Q = 2.0188 and $\omega_o$ = 5.504 krad/sec
Angular cross-over frequency, $\omega_c = 2\times3.14\times f_c = 2\times3.14\times2.5\times10^3 = 1.57\times10^4$ rad/sec
We know for an uncompensated system, $G_c(s) = 1$
Uncompensated loop gain is given by,

$$T(s) = (V_g\times H)/V_m\times 1/(1+Ls/R+s^2LC)$$

$$T(s) = (15\times1)/2.4 \times /(1+150\times10^{-6}s/1.667+s^2150\times10^{-6}\times220\times10^{-6}).$$

Fig 4 shows the bode plot of uncompensated loop gain of the system. Since phase margin required for compensated system is required to be 60˚, phase boost is required at gain crossover frequency. For uncompensated system, Phase margin (PM) at gain crossover frequency,

$$PM = 180^\circ - 169^\circ = 11^\circ$$

Thus, phase boost ($\theta$) of $60^{\circ}$ - $11^{\circ}$ = $49^{\circ}$ is required. So, the Type-3 compensator will be designed according to these parameters. Here, $f_c$ = 2.5 kHz, $\theta = 49^{\circ}$ and gain of 1.34 dB or 1.668 at $f_c$ = 2.5 kHz.

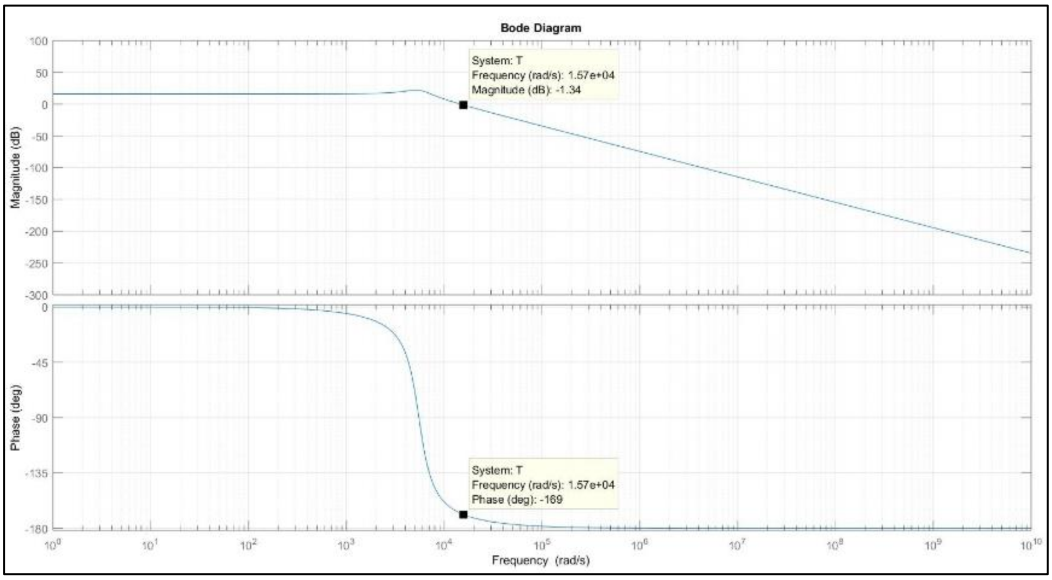


**Fig. 4.** Bode plot of loop gain of uncompensated system

Using the design equations given in reference [2],

Zero frequency,

$$f_z = f_c((1-sin(\theta))/(1+sin(\theta))\text{^}0.5)$$

$$f_z = f_c((1-sin(49))/(1+sin(49))\text{^}0.5)$$

$$f_z = 2.5\times10^3((1-sin(49))/(1+sin(49))\text{^}0.5) = 660.5285\ Hz,$$

$$\omega_z = 2\times3.14\times f_z = 4.1502\ krad/sec$$

Pole frequency,

$$f_p = f_c((1+sin(\theta))/(1-sin(\theta))\text{^}0.5)$$

$$f_p = f_c((1+sin(49))/(1-sin(49))\text{^}0.5)$$

$$f_p = 2.5\times10^3((1+sin(49))/(1-sin(49))\text{^}0.5) = 9462.1\ Hz,$$

$$\omega_p = 2\times3.14\times f_p = 59.452\ krad/sec$$

DC gain of the compensator,

$$G_{co} = (f_z/\ f_p)\text{^}0.5\times10\text{^}(1.34/20) = 0.3064$$

For removing switching frequency noises, we will put high frequency pole at $10\times f_c$. So, high frequency pole, $f_{hp}$= $10\times f_c$ = 25 kHz, $\omega_{hp}$= $2\times3.14\times f_{hp}$ = $1.57 \times 10^5$ rad/sec.

First zero frequency, $f_{z1} = f_c/10 = 250$ Hz, $\omega_{z1} = 2\times3.14\times f_{z1} = 1.57$ krad/sec.
Pole at origin frequency, $f_{po} = G_{co} \times f_{z1} = 76.6$ Hz, $\omega_{po} = 2\times3.14\times f_{po} = 481.5$ rad/sec.
Transfer function of Type-3 compensator,

$$G_c(s)=(G_{co}(1+s/\omega_z)(1+s/\omega_{z1}))/(s/\omega_{z1}(1+s/\omega_p)(1+s/\omega_{hp}))$$

$$= (G_{co}\omega_p\omega_{hp})/\omega_z \times ((\omega_z+s)(\omega_{z1}+s))/(s(\omega_p+s)(\omega_{hp}+s))$$

The loop gain of compensated system is,

$$T(s) = G_c(s)H(s)G_{PWM}(s)G_{vd}(s)$$

Since the system is unity feedback, H(s) = 1,

$$T(s) = G_c(s)G_{PWM}(s)G_{vd}(s)$$

Fig. 5 shows bode plot of designed Type-3 compensator transfer function along with equivalent Lead compensator transfer function. Fig. 6 shows bode plot of loop gain of the compensated system with Type-3 compensator confirming phase margin of 60˚ at gain cross over frequency of 2.5 kHz.

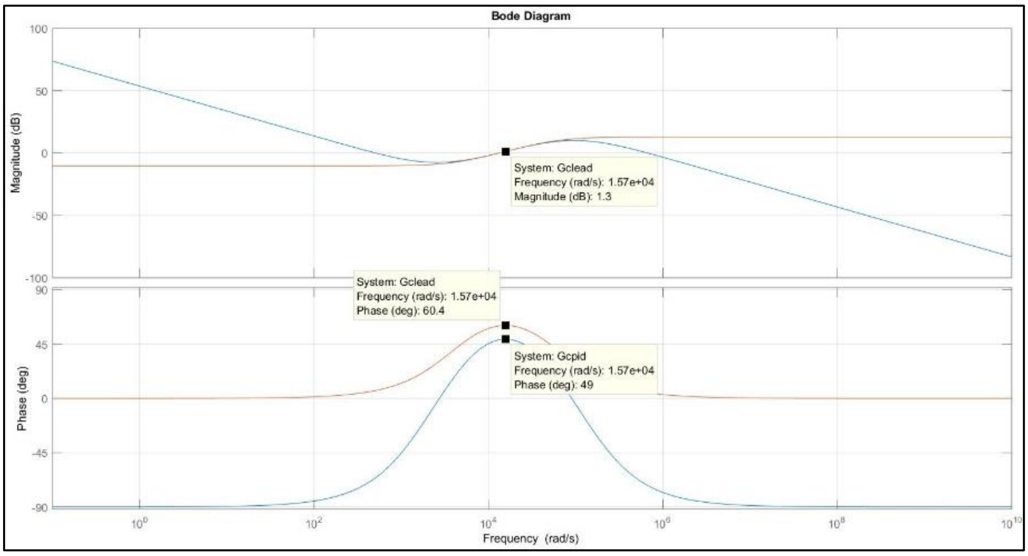


**Fig. 5.** Bode plot of equivalent Lead and Type-3 compensator

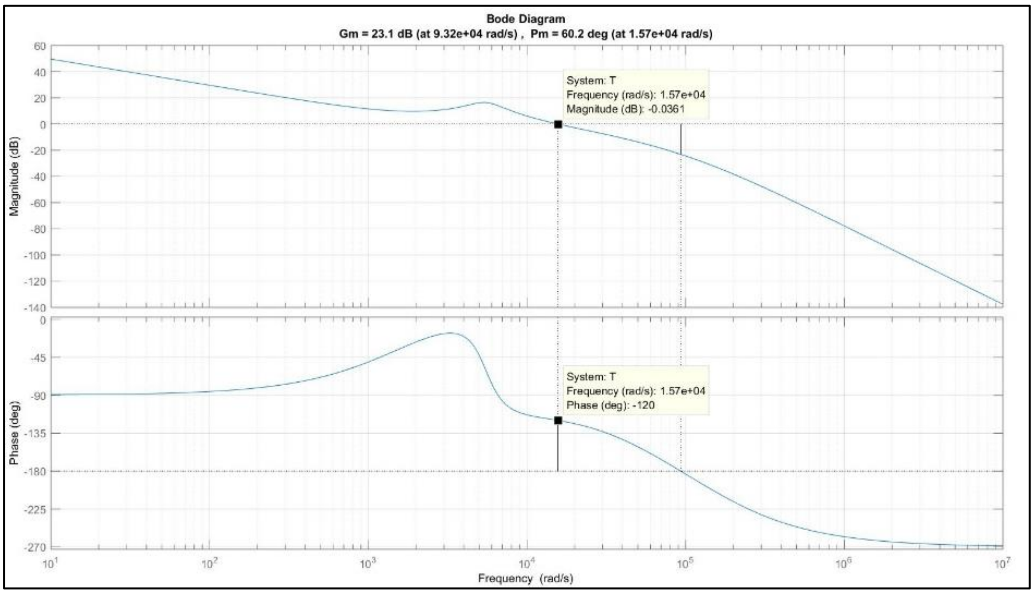


**Fig. 6.** Bode plot of loop gain of compensated system

### 3.2 Implementation of Type-3 compensator using op amp

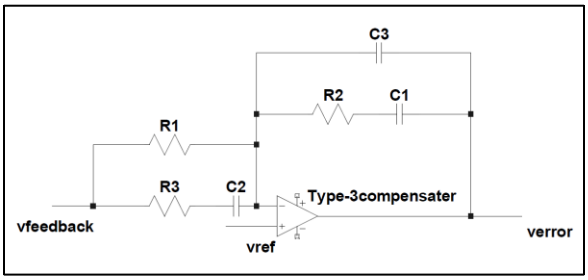


**Fig. 7.** Type-3 compensator using op amp

Using the following relations [6], we will find the values of required resistances and capacitance.

Let $R_1$=100 kΩ

$$C_1 = (f_{hp}-f_z)/(2\pi R_1 f_{po} f_{hp})$$

$C_1$ = 20.2 nF (selected value (10 nF + 10 nF) = 20 nF)

$$C_2 = (f_p-f_{z1})/(2\pi R_1 f_p f_{z1})$$

$C_2$ = 6.2 nF (selected value (3.3 nF + 3.3 nF) =6.6 nF)

$$C_3 = f_z/(2\pi R_1 f_{po} f_{hp})$$

$C_3$ = 540 pF (selected value 470 pF)

$$R_2 = (R_1 f_{po} f_{hp})/((f_p - f_z) f_z)$$

$R_2$ = 11.9 kΩ (selected value 12 kΩ)

$$R_3 = (R_1 f_{z1})/(f_p - f_{z1})$$

$R_3$ = 2.71 kΩ (selected value 2.7 kΩ)

### 3.3 Circuit Diagrams

The detailed circuit diagram used for implementation of power board, control board and driver board of the laboratory prototypes of close loop voltage mode controlled Buck converter operating at switching frequency of 25 kHz are shown in Fig 8. The list of their key components is given in Table 2, Table 3 and Table 4 respectively.

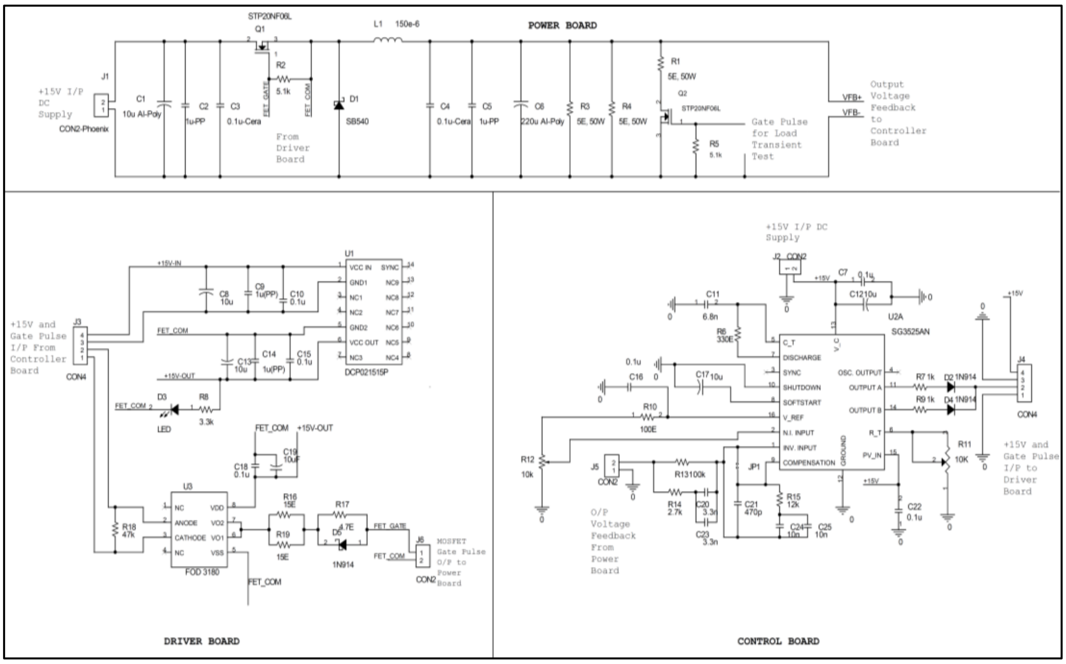


**Fig. 8.** Detailed circuit diagram of developed lab prototype of power board(top), control board (bottom right) and driver circuit ( bottom left)

Because of the floating source of the Buck converter MOSFET switch, isolated gate driver is required, which is implemented using Opto-coupler based gate driver IC FOD3180 [7] and isolated supply on the MOSFET side is obtained by IC DCP021515P [8]. Controller circuit is implemented using PWM controller IC SG3525AN [9] as shown in the diagram. Fig. 9 shows the developed laboratory prototype of the Buck converter with all subsystems.

**Table 2.** Components List for Power Board

| S. No. | Component Description | Quantity |
|---|---|---|
| 1 | MOSFET Switch (STP20NF06L) | 2- Nos. |
| 2 | Inductor (150 µH – 31 turns on toroidal core - HF1061252) | 1 - No |
| 3 | Schottky Diode (SB540) | 1 - No |
| 4 | Al Polymer Capacitor (220 µF, 16 V) | 1 - No |
| 5 | Polypropylene Capacitor (1 µF, 63 V) | 2- Nos. |
| 6 | Al Polymer Capacitor (10 µF, 25 V) | 1 - No |

**Table 3.** Components List for Driver Board

| S. No. | Component Description | Quantity |
|---|---|---|
| 1 | Optocoupler Gate Driver IC (FOD3180) | 1 - No. |
| 2 | Isolated DC-DC Converter IC (DCP021515P) | 1- No. |
| 3 | Fast Recovery Diode (1N914) | 1 - No. |
| 4 | Ceramic Capacitor (0.1 µF, 63 V) | 3 - Nos. |
| 5 | Polyester Capacitor (1 µF, 63 V) | 2 - Nos. |
| 6 | Electrolytic Capacitor (10 µF, 25 V) | 2 - Nos. |

**Table 4.** Components List for Control Board

| S. No. | Component Description | Quantity |
|---|---|---|
| 1 | PWM Controller IC (SG3525AN) | 1 - No. |
| 2 | Fast Recovery Diode (1N914) | 2 - Nos. |
| 3 | Polyester Capacitor (3.3 nF, 63 V) | 2 - Nos. |
| 4 | Polyester Capacitor (10 nF, 63 V) | 2 - Nos. |
| 5 | Polyester Capacitor (6.8 nF, 63 V) | 1- No. |
| 6 | Polyester Capacitor (470 pF, 63 V) | 1 – No. |
| 7 | Electrolytic Capacitor (10 µF, 25 V) | 2 - Nos. |

**Fig. 9.** Laboratory prototype of the Buck converter.

### 3.4 Experimental Results

The developed prototype of closed loop controlled Buck converter is thoroughly tested on resistive load for steady state as well as dynamic performance and following experimental waveforms are obtained. Fig. 10 shows key waveforms of the buck converter operating in steady state continuous current conduction mode while delivering load current of 3 A at regulated output voltage of 5 V. Load transient test is also performed on the converter to verify close loop stable operation as well as dynamic performance. Fig. 12 shows the waveforms of output voltage and inductor current during 1 A of step change in load current. Fig. 11 shows magnified view of output voltage undershoot when step load of 1 A is applied on the converter. Fig. 13 depicts magnified view of output voltage overshoot when step load of 1 A is removed. In both cases, following the transient, output voltage reaches final value promptly without oscillations, verifying proper controller design and stable operation of control loop of the Buck converter.

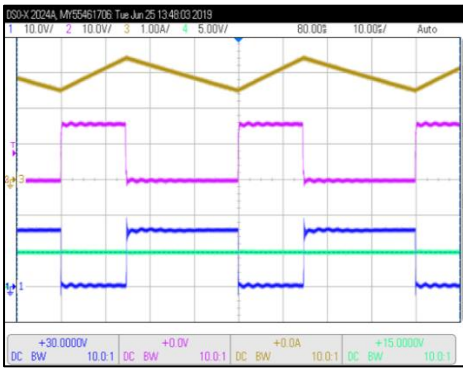

**Fig. 10.** Waveforms (from top) of inductor current, MOSFET gate-source voltage, MOSFET drain-source voltage and output voltage.

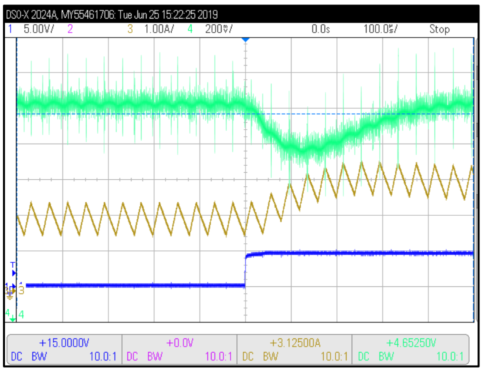

**Fig. 11**. Waveforms of output voltage (top), inductor current (middle) and load current (bottom) when 1 A of step load is applied.

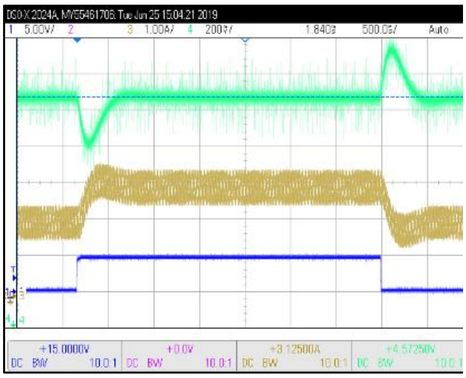

**Fig. 12.** Load transient waveforms for 1 A step change in load current: output voltage (top), inductor current (middle), load current (bottom).

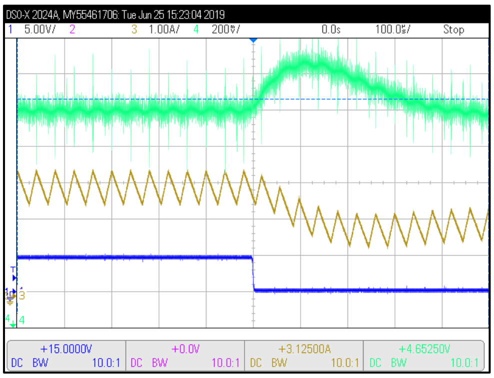

**Fig. 13**. Waveforms of output voltage (top), inductor current (middle), load current (bottom) when 1 A of step load is removed.

## 4 Conclusion

Design oriented study of Buck converter compensator design was carried out for their operation under continuous current conduction mode in closed loop voltage mode control. Lead compensator was attempted first but it suffered from non-zero steady state error though it provided required crossover frequency and phase margin. Therefore, a Type-3 controller was designed and implemented using op amp present in the PWM controller IC SG3525AN The Optocoupler gate driver IC FOD 3180 is used to drive the MOSFET switch. The bode plots of control to output transfer function, loop gain (compensated and uncompensated) were plotted and verified for achievement of required phase margin and gain cross over frequency. Buck converter was implemented on hardware in the lab. Testing of the developed converter was carried out and proper close loop stable operation of the converter was verified with satisfactory dynamic as well as steady state performance.

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