EasyChair Preprint

№ 10551

Novel Switched-Capacitor DC-DC Converter Achieving Highest Rational Conversion Ratios Using Inter-Stage Feedback

Nagesh Patle and Bibhu Datta Sahoo

July 13, 2023

Novel Switched-Capacitor DC-DC Converter Achieving Highest Rational Conversion Ratios Using Inter-Stage Feedback

Nagesh Patle
Dept. of Electrical Engineering and Computer Sciences
University of California, Berkeley
Berkeley, USA
nageshpatle@berkeley.edu

Bibhu Datta Sahoo
Dept. of Electronics and Electrical Communication Engg
Indian Institute of Technology Kharagpur
Kharagpur, India
bsahoo@ieee.org

***Abstract*—This paper proposes an inter-stage feedback-based switched-capacitor (IFSC) converter that can be configured to realize any rational voltage-conversion ratio (VCR) using a minimum number of 2:1 switched-capacitor (SC) stages. The converter enables efficient dynamic voltage scaling (DVS) operation over a larger voltage range by significantly increasing the resolution of voltage levels. Additionally, a restructuring algorithm has been proposed to achieve all VCRs without requiring any additional dedicated voltage stages. The converter extends the idea of the recursive switched-capacitor (RSC) topology, which spans 2^N-1 ratios with N 2:1 SC cells. Comparative analysis shows that the proposed converter outperforms the negative-output feedback-based converter in terms of bottom-plate parasitic loss for most VCRs. To validate the concept, a fully-reconfigurable hardware prototype has been developed.**

***Index Terms*—dc-dc converter, reconfigurable switched capacitor converter, inter-stage feedback, recursive converter**

I. Introduction

Modern digital system-on-chips (SoCs) trade off power consumption and performance through dynamic voltage scaling (DVS). Although linear regulators can achieve DVS with fine granularity and fast response times, their efficiency is poor, thereby significantly compromising the system-level energy efficiency. Off-chip inductor-based switching converters can generate continuous voltage levels with high conversion efficiency through pulse width modulation-based regulation. However, their use of large inductors results in slow response times, thus posing challenges in the implementation of fast DVS control loops [1]. In addition, off-chip inductors also adversely affect the system performance in RF/analog-mixed signal systems, leading to increased overall system cost. Integrating on-chip inductors require a high Q-factor for good efficiency, necessitating special masks and increased manufacturing costs [2], [3].

Switched-capacitor converters (SCCs) emerged as favorable candidates to facilitate DVS due to compatibility with integrated processes, faster voltage conversion ratio (VCR) control, and high efficiency at multiple voltage levels [1], [4]. However, most SCCs achieve high efficiency only close to discrete voltage levels through frequency modulation while having a low-efficiency valley between two voltage levels. SCCs that offer multiple VCRs have finer granularity and facilitate efficient DVS for larger voltage ranges.

Recursive switched-capacitor (RSC) [5]–[7] and successive-approximation switched-capacitor (SAR) [2], [8], [9] topologies were proposed to enable high efficiency across wide voltage range by providing 2^N-1 VCRs using N 2:1 SC stages. Negative-output feedback-based switched-capacitor (NSC) topology [10], [11] increases the VCR count to any rational-conversion ratio ($O(4^N)$) by using voltage negators (See Table I). This topology achieves reduced conduction loss, however, at the cost of an increased number of large reconfiguration switches. Moreover, the voltage swing of the same node from $-V_{out}$ to $2V_{in}-V_{out}$ requires complex switch protection schemes and results in higher bottom-plate parasitic loss and high switching losses at the gate drivers during DVS [12].

Fig. 1 summarises the general architectures of RSC, SAR, and NSC topologies, along with the structure of the 180^o-interleaved 2:1 SC stage which performs the averaging operation of its two inputs in all these topologies. For RSC and SAR topologies, $VCR{=}A/2^N$ and $a_N \dots a_1$ are the binary weights of the N-bit binary input control signal A. For NSC topology $VCR{=}A/(2^{N-1}{+}B)$, and $a_N \dots a_1$ & $b_N \dots b_1$ represent the binary weights of the N-bit binary input control signals A and B respectively.

TABLE I: Realizable VCR count in 2:1 SC stage-based reconfigurable SCC topologies.

Max no. of stages		2	3	4	5	6	N
VCR Count	RSC/SAR	3	7	15	31	63	2^N-1
	NSC/IFSC	5	21	79	323	1259	$O(4^N)$

This paper is organized as follows. Section II introduces the architecture of the inter-stage feedback-based switched-capacitor (IFSC) topology and stage restructuring algorithm.

Nagesh Patle was affiliated with Dept. of E&ECE, Indian Institute of Technology Kharagpur, Kharagpur-721302, INDIA, when this research was undertaken.

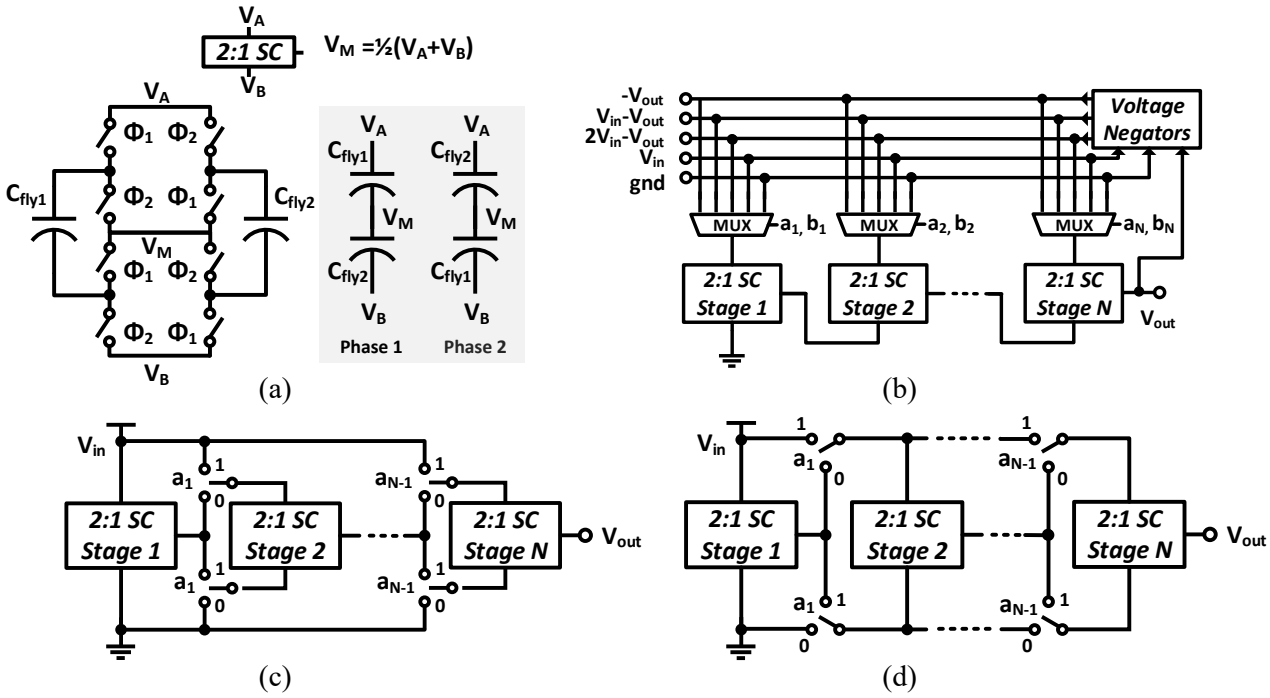


Fig. 1: (a) 180^o-interleaved 2:1 SC Stage (b) NSC topology (c) RSC topology (d) SAR topology.

In section III, the conventional reconfigurable SC topologies are compared with IFSC topology on the metrics of conduction loss and bottom-plate parasitic loss. Section IV presents the circuit-level implementation of the general 2:1 SC stage-based reconfigurable SC topology. In Section V, measurement results are presented. Section VI concludes the paper.

II. Proposed Inter-stage Feedback Topology

Fig. 2 shows the general architecture of the proposed IFSC topology. The core idea is to interconnect the terminals of N 2:1 SC stages in such a manner that any rational conversion ratio p/q can be realized such that $1 \leq p < q \leq 2^N$. Most of the ratios only need either V_{in}, V_{out} or gnd as the inputs for the stages, however, some ratios demand inter-stage outputs to be made available for restructuring as discussed later in this section.

As discussed later in Section III, the proposed IFSC topology surpasses the NSC topology to attain the highest number of VCRs per SC stage as it can generate the same number of ratios with N 2:1 stages but the NSC topology requires $(N-1)$ 2:1 SC stages and 2 negator stages. Since both NSC and IFSC topologies converge to the RSC topology configuration for VCRs with denominators as powers of 2, they can both be seen as rational conversion extensions to RSC, where NSC uses negative feedback while IFSC implements positive and inter-stage feedback. It is worth noting that, all the internal node voltages in IFSC are always bounded within V_{in} and gnd, whereas, in NSC, the nodes can swing between $2V_{in} - V_{out}$ and $-V_{out}$.

From Section IV, it has been shown that the reconfiguration switch count is significantly reduced in IFSC as compared to NSC topology.

Fig. 3 shows the configurations of 2:1 SC-based reconfigurable SCCs for achieving a target VCR of 0.26.

This section will elaborate on the synthesis of IFSC topology from the target ratio information and will further discuss how to handle special VCR cases through restructuring.

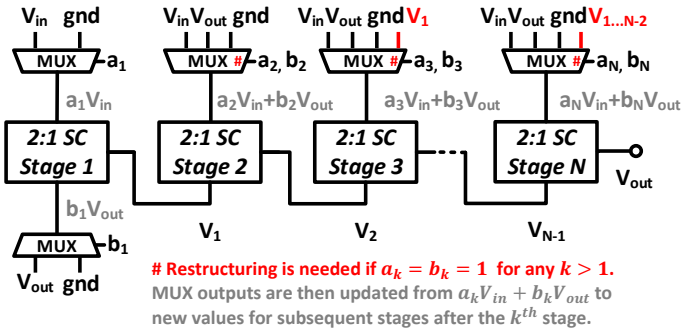
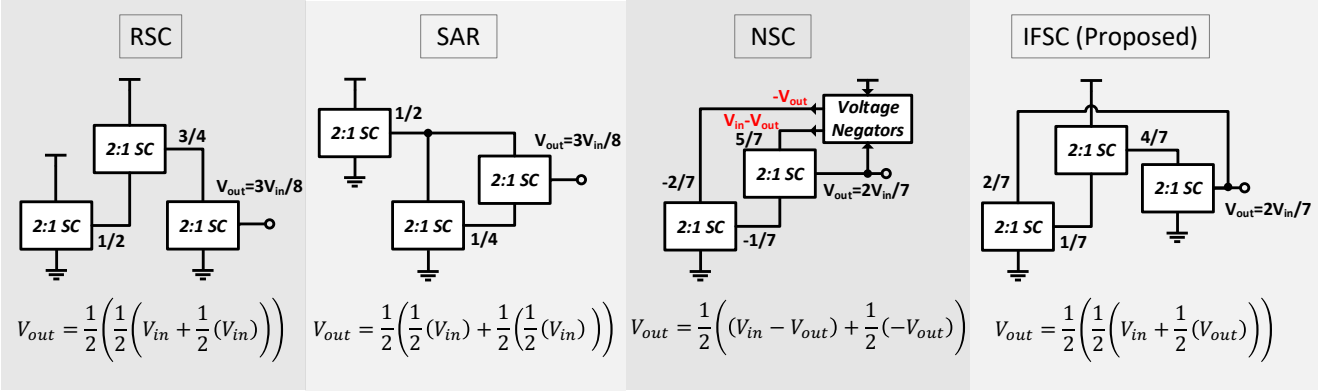


Fig. 2: General architecture of the proposed IFSC topology.

A. Mathematical Formulation

For a target VCR of p/q, we start with the primary formulation where V_{out} is determined by the weighted sum of V_{in} and itself as depicted in (1):

$$V_{out} = \frac{A}{2^N} V_{in} + \frac{B}{2^N} V_{out} \tag{1}$$



(a) (b) (c) (d)

Fig. 3: Configuration of reconfigurable SCCs for a target VCR of 0.26. The nearest achievable VCRs have been realized: $3/8 \approx 0.375$ for RSC and SAR and $2/7 \approx 0.286$ for NSC and IFSC. A closer VCR to the target implies lesser voltage conversion required from the linear regulator, thus maximizing the overall efficiency of the SCC-Linear Regulator system.

Here, $A/2^N$ represents the forward path gain and $B/2^N$ denotes the positive feedback factor. The lowest N, which also represents the bit-depth or the number of 2:1 stages required, is chosen such that $2^N \geq q$. It is followed by the equivalent binary decomposition of A and B, represented as follows:

$$VCR = \frac{V_{out}}{V_{in}} = \frac{A}{2^N - B} \equiv \frac{(0.a_N a_{N-1} \dots a_2 a_1)_2}{1 - (0.b_N b_{N-1} \dots b_2 b_1)_2} \quad (2)$$

Here, $a_N \dots a_1$ and $b_N \dots b_1$ are the binary weights of N-bit input control signals A and B, respectively. To understand how these control signals configure a particular VCR, the expression in (1) can be expanded further as shown in (3).

$$\begin{aligned} V_{out} &= \sum_{i=1}^{N} \frac{2^{i-1}a_i}{2^N} V_{in} + \sum_{i=1}^{N} \frac{2^{i-1}b_i}{2^N} V_{out} \\ &= \sum_{i=1}^{N} \frac{a_i}{2^{N+1-i}} V_{in} + \sum_{i=1}^{N} \frac{b_i}{2^{N+1-i}} V_{out} \\ &= \left(\frac{a_N}{2} + \dots + \frac{a_1}{2^N}\right) V_{in} + \left(\frac{b_N}{2} + \dots + \frac{b_1}{2^N}\right) V_{out} \\ &= \frac{1}{2}\Bigg((a_N V_{in} + b_N V_{out}) + \frac{1}{2}\Bigg((a_{N-1} V_{in} + b_{N-1} V_{out}) + \\ &\quad \dots + \frac{1}{2}\Big((a_1 V_{in} + b_1 V_{out})\Big)\Bigg)\Bigg) \end{aligned} \quad (3)$$

The formulation obtained can be seen as the recursive cascading of N $2:1$ SC stages where the i^{th} stage produces an average of $a_i V_{in} + b_i V_{out}$ and the output of the $(i-1)^{th}$ stage, as depicted in Fig. 2. It is important to note here that $a_i V_{in} + b_i V_{out}$ can have four values: V_{in}, V_{out}, gnd and $(V_{in} + V_{out})$ depending on the control signal bits a_i and b_i. However, the proposed topology does not have an additional stage to generate $(V_{in} + V_{out})$. In such a case, whenever, $a_i = b_i = 1$ for any i in the primary formulation, we need to find ways to restructure our connections to obtain the final restructured representation.

Algorithm 1 Stage Input Restructuring Algorithm

```
for i = N to 2 do
    if a_i = b_i = 1 then
        input (i) ⇐ (a_i − a_1)V_in + (b_i − b_1)V_out
        input (gid) ⇐ V_{gid−i}
    end if
    if input (i) is gnd then
        gid ⇐ i
    end if
end for
```

TABLE III: Algorithm 1 Implementation for VCR=3/5 & 7/13.

3/5	S1	S2	S3	7/13	S1	S2	S3	S4
Primary Representation (at $i=3$)				Primary Representation (at $i=4$)				
V_A	V_{in}	$V_{in}+V_{out}$	gnd	V_A	V_{in}	$V_{in}+V_{out}$	V_{in}	gnd
V_B	V_{out}	V_1	V_2	V_B	V_{out}	V_1	V_2	V_3
Restructured Representation (at $i=2$)				Restructured Representation (at $i=2$)				
V_A	V_{in}	gnd	V_1	V_A	V_{in}	gnd	V_{in}	V_2
V_B	V_{out}	V_1	V_2	V_B	V_{out}	V_1	V_2	V_3

B. Stage Input Restructuring

For most VCRs in an N-stage IFSC topology, the primary formulation is sufficient to enable the designer to obtain the final structure. In fact, the restructuring is not needed for 19 VCRs out of 21 discrete VCRs in 3-stage and for 40 VCRs out of 79 discrete VCRs in 4-stage[1] IFSC topology. If the designer wishes to minimize the number of reconfiguration switches, the remaining VCRs can be skipped, while compromising the full realizability potential of the proposed topology.

A stage restructuring methodology has been discussed in Algorithm 1 which enables the designers to realize all remaining VCRs without requiring any additional stage. The main idea here is to identify and strategically reuse the available outputs

[1]While the IFSC topology can realize all the 4-bit VCRs, VCR=7/10 needs an additional step which is skipped for the brevity of the discussion.

TABLE II: Summary of realizations of all VCRs upto 3-bit using the proposed IFSC method

Ratio No.	p	q	Stage-1 V_A	Stage-1 V_B	Stage-2 V_A	Stage-2 V_B	Stage-3 V_A	Stage-3 V_B	V_{out}	Realizability RSC	Realizability SAR	Realizability NSC
1	1	8	V_{in} (1)	gnd (0)	V_1 (0.5)	gnd (0)	V_2 (0.25)	gnd (0)	0.125	✓	✓	✓
2	1	7	V_{in} (1)	V_{out} (0.143)	V_1 (0.571)	gnd (0)	V_2 (0.286)	gnd (0)	0.143	×	×	✓
3	1	6	V_{in} (1)	gnd (0)	V_1 (0.5)	V_{out} (0.167)	V_2 (0.333)	gnd (0)	0.167	×	×	✓
4	1	5	V_{in} (1)	V_{out} (0.2)	V_1 (0.6)	V_{out} (0.2)	V_2 (0.4)	gnd (0)	0.200	×	×	✓
5	1	4	V_{in} (1)	gnd (0)	V_1 (0.5)	gnd (0)	-	-	0.250	✓	✓	✓
6	2	7	gnd (0)	V_{out} (0.286)	V_1 (0.143)	V_{in} (1)	V_2 (0.571)	gnd (0)	0.286	×	×	✓
7	1	3	V_{in} (1)	V_{out} (0.333)	V_1 (0.667)	gnd (0)	-	-	0.333	×	×	✓
8	3	8	V_{in} (1)	gnd (0)	V_1 (0.5)	V_{in} (1)	V_2 (0.75)	gnd (0)	0.375	✓	✓	✓
9	**2**	**5**	gnd (0)	V_{out} (0.4)	V_1 (0.2)	V_{in} (1)	V_2 (0.6)	V_1 (0.2)	0.400	×	×	✓
10	3	7	V_{in} (1)	V_{out} (0.428)	V_1 (0.714)	V_{in} (1)	V_2 (0.857)	gnd (0)	0.428	×	×	✓
11	1	2	V_{in} (1)	gnd (0)	-	-	-	-	0.500	✓	✓	✓
12	4	7	gnd (0)	V_{out} (0.571)	V_1 (0.286)	gnd (0)	V_2 (0.143)	V_{in} (1)	0.571	×	×	✓
13	**3**	**5**	V_{in} (1)	V_{out} (0.6)	V_1 (0.8)	gnd (0)	V_2 (0.4)	V_1 (0.8)	0.600	×	×	✓
14	5	8	V_{in} (1)	gnd (0)	V_1 (0.5)	gnd (0)	V_2 (0.25)	V_1 (1)	0.625	✓	✓	✓
15	2	3	gnd (0)	V_{out} (0.667)	V_1 (0.333)	V_{in} (1)	-	-	0.667	×	×	✓
16	5	7	V_{in} (1)	V_{out} (0.714)	V_1 (0.857)	gnd (0)	V_2 (0.428)	V_{in} (1)	0.714	×	×	✓
17	3	4	V_{in} (1)	gnd (0)	V_1 (0.5)	V_{in} (1)	-	-	0.750	✓	✓	✓
18	4	5	gnd (0)	V_{out} (0.8)	V_1 (0.4)	V_{out} (0.8)	V_2 (0.6)	V_{in} (1)	0.800	×	×	✓
19	5	6	V_{in} (1)	gnd (0)	V_1 (0.5)	V_{out} (0.833)	V_2 (0.667)	V_{in} (1)	0.833	×	×	✓
20	6	7	gnd (0)	V_{out} (0.857)	V_1 (0.428)	V_{in} (1)	V_2 (0.714)	V_{in} (1)	0.857	×	×	✓
21	7	8	V_{in} (1)	gnd (0)	V_1 (0.5)	V_{in} (1)	V_2 (0.75)	V_{in} (1)	0.875	✓	✓	✓

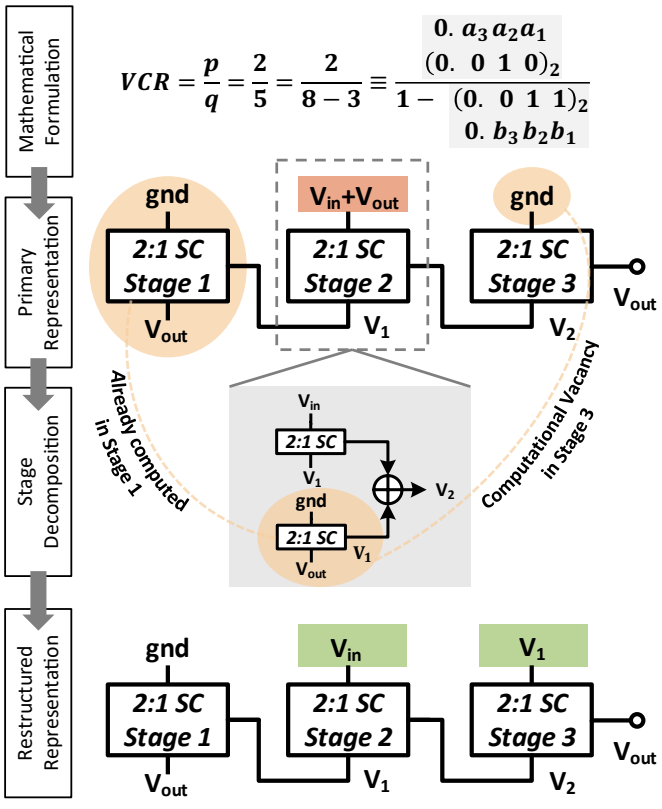


Fig. 4: Stage input restructuring example for $VCR = 2/5$ realized using IFSC topology.

from the previous stages for the next stages. Table III demonstrates the implementation of the algorithm for two different VCRs which require restructuring. Figure 4 demonstrates the idea of reuse for VCR=2/5, where the concerned stage can be decomposed into the sum of the pre-computed stage and a new stage. While the new stage replaces the existing stages, the pre-computed stage output is forwarded to a future stage that has gnd as its input. The algorithm takes advantage of the fact that if an averaged output is thought of as a sum of two halved outputs, then gnd on one of its terminals is redundant and thus can be treated as a computational vacancy.

Table II summarizes the implementations for all the VCRs realized with the IFSC topology with a maximum of three 2:1 SC stages. Except for $VCR = 2/5$ and $3/5$, the rest of the VCRs are obtained directly from primary formulation without the need for restructuring. While NSC topology can also realize all these ratios, RSC and SAR can only attain the ratios with the denominator as a power of 2.

III. Comparison of Reconfigurable Topologies

Conduction loss, bottom-plate parasitic loss, and steady-state response of all the reconfigurable topologies is discussed in this section.

A. Analysis of Conduction Loss

The intrinsic conduction losses in a switched-capacitor converter during voltage conversion are modeled with an output impedance (R_{eq}) [13], [14]. The conduction losses can be attributed to losses due to charge transfer between capacitors, modeled by *slow-switching limit impedance* (R_{SSL}), and losses due to switches, modeled by *fast-*

switching limit impedance (R_{FSL}) as shown in (4).

$$R_{SSL} = \sum_i \frac{a_{c,i}^2}{C_i f_{sw}}, R_{FSL} = 2\sum_j R_j a_{r,j}^2 \tag{4}$$

Here, $a_{c,i}{=}q_{c,i}/q_{out}$ and $a_{r,j}{=}q_{r,i}/q_{out}$ denote the charge multiplier coefficient for the i^{th} capacitor and j^{th} switch respectively. C_i represents the value of the i^{th} capacitor. R_j represents the on-resistance of the j^{th} switch. The ESR of the capacitors and the reconfiguration switches are not being considered in the R_{FSL} expression for the sake of simplicity of analysis. Interestingly, if the 2:1 SC stage is implemented with 180^o-interleaved stages as depicted in Fig. 1(a), certain simplifications can be made. Charge multiplier coefficients of both the flying capacitors and all 8 switches are equal to each other in a 2:1 SC stage. Let us define a_k as the charge multiplier coefficient for the k^{th} SC stage, thus $a_k{=}a_{c,i}{=}a_{r,j}$, given that i, j, and k belong to the same stage. Figure 5 demonstrates the charge flow through each stage for $VCR = 2/5$ and $2/7$ realized using the IFSC topology. The corresponding a_k vectors would be $1/5\begin{bmatrix}3 & 2 & 4\end{bmatrix}$ and $1/7\begin{bmatrix}1 & 2 & 4\end{bmatrix}$, respectively.

In order to have a fair comparison between the various reconfigurable topologies, their stages have to be sized optimally under the same constraints. Based on the analysis done in [13], the optimal expressions for R_{SSL} and R_{FSL} is given by (5) under the constraints of constant total capacitance (C_{tot}) and total switch conductance (G_{tot}), assuming that all the capacitors and switches are rated for an identical voltage.

$$R^*_{SSL} = \frac{2}{C_{tot} f_{sw}}\Big(\sum_k |a_k|\Big)^2, R^*_{FSL} = \frac{4}{G_{tot}}\Big(\sum_k |a_k|\Big)^2 \tag{5}$$

The topology that has lower $\sum_k |a_k|$ for a given VCR, will minimize both the R_{SSL} and R_{FSL}, thereby minimizing the overall conduction loss at any switching frequency.

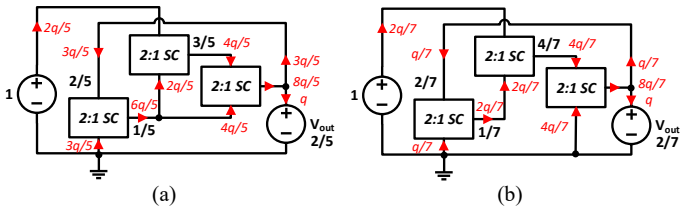
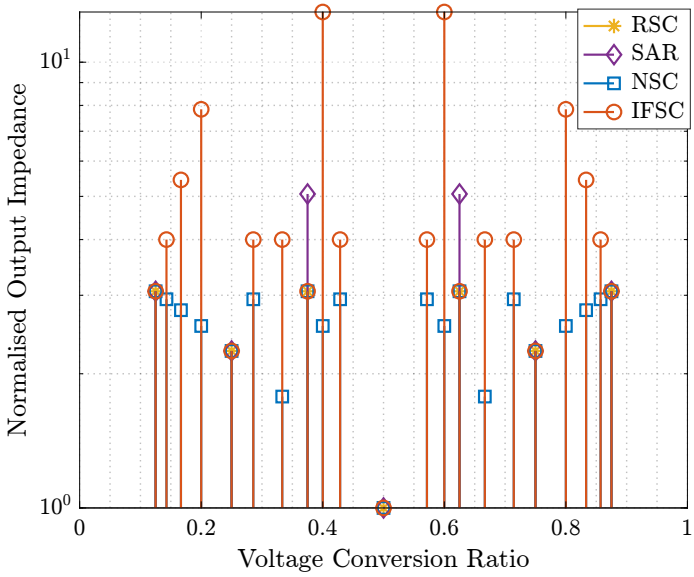


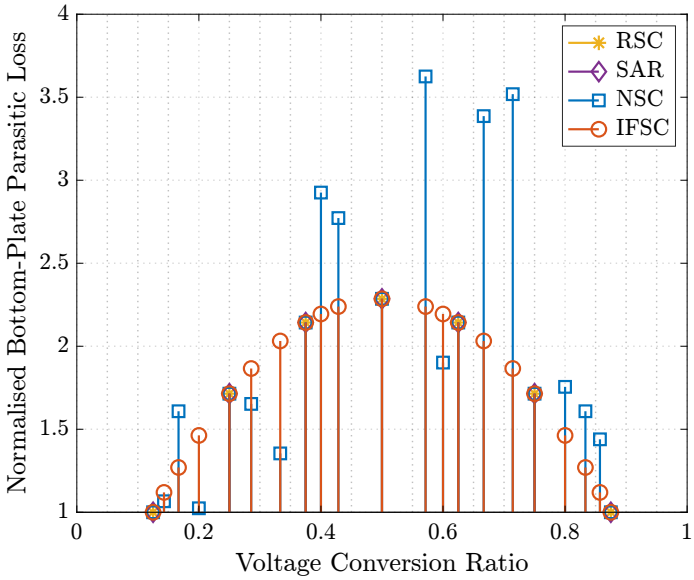
Fig. 5: Charge flow through the 2:1 SC cells for VCR realizations with IFSC topology. (a) VCR=2/5. (b) VCR=2/7.

B. Analysis of Bottom-Plate Parasitic Loss

In integrated applications, there is an inherent loss associated with the parasitic capacitance between the bottom metal plate and the substrate caused by the switching of the flying capacitors. Considering α as the ratio between the parasitic capacitance and the flying capacitance (C_i), $V_{C_i,bot}$ as the bottom-plate voltage swing, and f_{sw} as the switching



(a)



(b)

Fig. 6: Comparison of (a) Normalized conduction loss Vs VCR and (b) normalized bottom-plate parasitic loss Vs VCR for various reconfigurable topologies.

frequency, the expression for the bottom-plate parasitic loss can be written as:

$$P_{bot} = f_{sw}\Big(\sum_i \alpha C_i (\Delta V^2_{C_i,bot})\Big) \tag{6}$$

$$\propto \sum_i |a_k|(V_{A_k} - V_{B_k})^2 \tag{7}$$

Here, the α has been assumed to be a constant for a technology, thus it doesn't take part in the normalized expression. Moreover, C_i has been assumed to be chosen as per the conduction loss optimization analysis. V_{A_k} and V_{B_k} denote the rail voltages at two inputs of k^{th} SC stage. Note that such an optimization choice does not minimize the bottom-plate

parasitic loss.

All the reconfigurable topologies based on 2:1 SC stages have been compared on the metrics of normalized conduction loss and the normalized bottom-plate parasitic loss as shown in Fig. 6. There are two key takeaways: (i) the IFSC topology is a superior candidate for minimizing the bottom-plate parasitic loss for most VCRs while also providing the highest number of ratios with minimal stage count and (ii) IFSC topology has similar conduction loss when compared with RSC and SAR topologies, however, performing slightly worse when compared with NSC topology.

C. Steady-State Response

Figure 7 shows the time-domain waveforms for the RSC, SAR, NSC, and IFSC topologies at the steady state. The simulated results have been generated using PLECS with a total capacitance of $500\,\mu F$ optimally distributed among stages to minimize the conduction loss. During DVS operation, if these topologies were to realize a target voltage of $1.3\,V$ with V_{in}=$5\,V$, then the nearest voltage level NSC and IFSC topologies could theoretically achieve is $\approx 1.43\,V$ corresponding to a VCR of 2/7. However, the RSC and SAR topologies can only achieve $\approx 1.875\,V$ corresponding to a VCR of 3/8. The required reduction in voltage (V_{target}/V_{avg}) has been marked in Fig. 7. If the linear regulator is cascaded with SCCs for the voltage reduction, then the RSC and SAR are destined to observe a large reduction in efficiency ($> 25\%$) in addition to the SCC losses. However, the NSC and IFSC could enjoy a healthy ($> 90\%$) regulator efficiency, thanks to the high granularity of the rational VCRs.

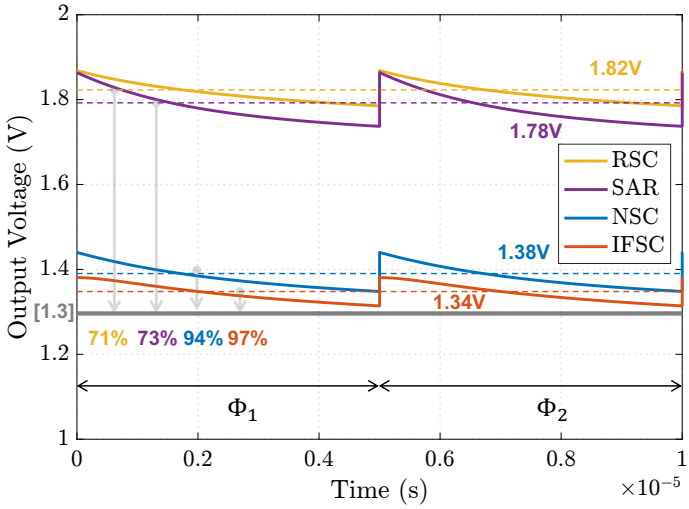


Fig. 7: Simulated steady-state output waveform of reconfigurable SCCs from Fig. 3 for a target V_{out} of $1.3\,V$ at f_{sw}=$100\,kHz, V_{in}$=$5\,V, I_{out}$=$5\,A, ESR$=$R_{ds}(on)$=$10\,m\Omega$, C_{out}=$1\,mF, C_{tot}$=$500\,\mu F$.

D. Comments on Process Implementation

Presence of $2V_{in}-V_{out}$ and $-V_{out}$ voltage rails in NSC topology necessitates deep N-well protection in the technology as they extend beyond the range of power supply rails V_{in} and gnd. It not only adds to the design complexity but also suggests increased gate driver switching losses. In addition, during ratio reconfiguration for DVS, some nodes might need to connect to $-V_{out}$ for one ratio and $2V_{in}-V_{out}$ for another, thus resulting in a required voltage change of $2V_{in}$, which statistically implies higher capacitor redistribution losses. On the contrary, the proposed IFSC topology gets rid of the concerning voltage rails and limits all nodes to always stay within power supply rails.

IV. Circuit Implementation

All the discussed reconfigurable SCCs use 2:1 SC stages as building blocks. The 3-terminals of the stage are expected to act as stiff voltage rails in the steady state with the relation $V_A > V_M > V_B$ (ref. Fig. 1(a)). Out of the 8 switches in the 180^o-interleaved stage (ref. Fig. 1(a)), the switches connecting the capacitor top plates to V_A and the bottom plate to V_M are realized using PMOS. Similarly, the remaining switches connecting the capacitor top plates to V_A and the bottom plate to V_M are realized using NMOS. Notably, the top unit of switches connected to top plates is identical to the bottom unit of switches connected to bottom plates and both these units can be realized using two H-bridge circuits operating with two-phase non-overlapping clock. These H-bridges are usually driven by gate drivers followed by cross-coupled bootstrapped circuits as discussed in [10].

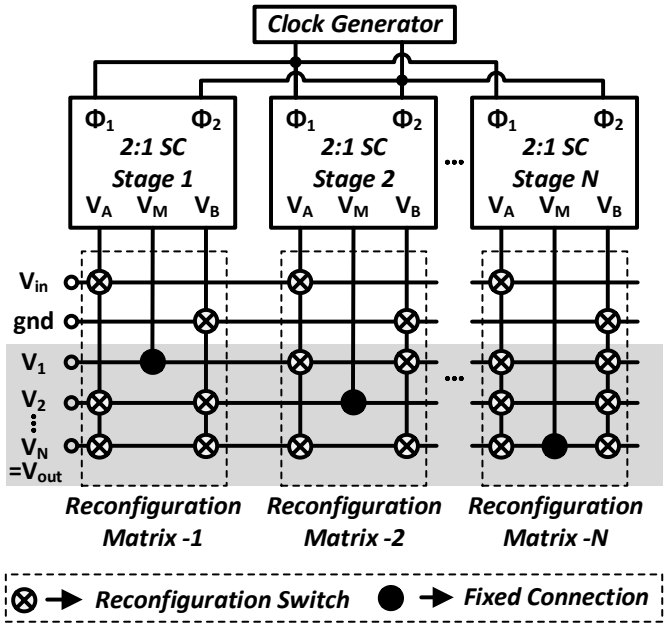


Fig. 8: Reconfigurable architecture to realize all VCRs with the proposed IFSC topology.

A. General Reconfigurable Architecture

Figure 8 shows the general architecture for realizing the IFSC topology with N 2:1 SC stages. The SC stages have been

redrawn to show the non-overlapping clock inputs coming from the clock generator to each block through an implicit gate driver. In order to realize all the VCRs during DVS operation, the 2:1 SC stage terminals should be reconfigurable to connect to multiple stiff voltage rails. Since V_A and V_B assume the highest and the lowest potentials in a 2:1 SC stage, V_{in} can only connect to V_A and gnd can only connect to V_B. The output terminal V_M of the k^{th} stage has a fixed connection to the V_k voltage rail. Since the voltage level of the intermediate nodes ($V_1 \dots V_N$) can assume any potential, two reconfiguration switches are assigned for each intermediate voltage rail per stage. The analog MUX in the block diagram in the general IFSC architecture (ref. Fig. 2) is equivalent to the reconfiguration matrix in the circuit implementation of Fig. 8, where exactly one of the power rails is connected to 2:1 SC stage terminals.

During the DVS operation of a microprocessor, based on the load performance requirement, a target VCR is selected from the lookup table and the feedback circuit generates the control signals for these reconfiguration switches.

B. Heuristic Design Strategies

The reconfigurable architecture of the IFSC topology achieves a significant hardware improvement as compared to the NSC topology [10] mainly for following three reasons:

- In NSC architecture, all the stages have 4-terminals to be able to be reconfigured as either a negator or a 2:1 SC stage as per VCR realization requirement. This requires one additional reconfiguration switch column per stage.
- 3 extra reconfiguration switch rows are needed to accommodate the interconnection with $-V_{out}, V_{in}-V_{out}$, and $2V_{in}-V_{out}$ voltage rails.
- All VCRs require different sizing of the capacitors for maximizing the conduction loss, thus necessitating (2^N-1) SC stages for optimal utilization of the overall capacitance.

On the contrary, IFSC topology requires only 3-terminal SC stages and no additional voltage rail. Most importantly, it can be designed with heuristic optimization in mind to minimize the reconfiguration switch overhead. For most of the VCRs, the flying capacitance distribution for optimal conduction loss is given by $1{:}2{:}4\dots2^N$ for N stages. The VCRs that require restructuring differ slightly in the optimal distribution, however, they can still achieve sub-optimal performance if they are scaled in the proportion $1{:}2{:}\dots{:}2^N$. Thus, a lot of hardware savings can be achieved for the reconfiguration switches if the stage components are always sized in the proportion $1{:}2{:}\dots{:}2^N$.

In addition, the reconfiguration switch count can be brought further down if the switches which realize the least number of VCRs are removed, while slightly compromising on the count of VCRs.

V. Hardware Prototype

A printed circuit board (PCB) prototype is constructed to verify the working of the proposed IFSC topology (Fig. 9). The fully reconfigurable design consists of five identical 2:1 4-terminal SC stages. It can be configured to realize up to 4-bit VCRs (Max. 79 distinct VCRs) for both the NSC and the proposed IFSC topology. A full component list is provided in Table IV. The circuit is implemented in an open loop and the different VCRs are attained with manual shorting of the corresponding reconfiguration matrix node, realized using double-row pin headers.

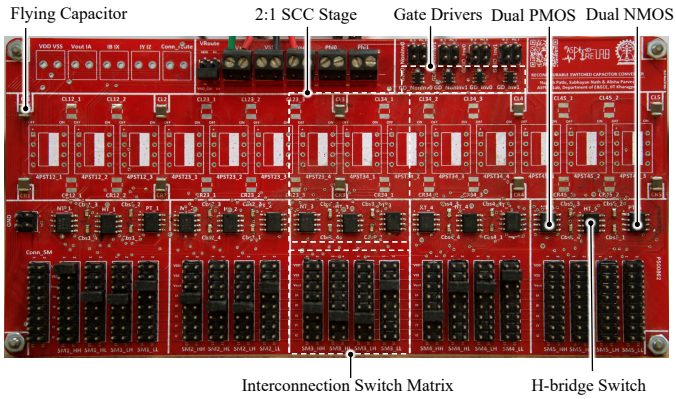


Fig. 9: Annotated photograph showcasing the PCB-based proof of concept design for a reconfigurable SCC, featuring five switched-capacitor stages.

TABLE IV: Component Listing for the PCB Prototype of the Reconfigurable Converter

Component	Parameters	Manuf./Part No.
Flying Capacitor	$47\mu F$	Taiyo Yuden JMK325BJ476KMHP
	$100\mu F$	Kemet T495D107K006ATE050
MOSFET H-Bridge	$R_p(on) = 80m\Omega$ $R_n(on) = 60m\Omega$	Diodes Inc. ZXMHC3F381N8
Output Capacitor	$680\mu F$	Kemet TPSE687K006R0060
Bootstrap Capacitor	$0.01\mu F$	AVX 06035C104JAT2A
Boostrap Dual NMOS	$R_n(on) = 4.7m\Omega$	Vishay SI4204DY-T1-GE3
Boostrap Dual PMOS	$R_p(on) = 19m\Omega$	Infineon IRF9358TRPBF
Gate Driver	14V, Inv/Non-inv	TI LM5134BMF/NOPB

Since the components in all the stages are sized identically, the expression for optimal conduction loss discussed in Section III is not applicable. Equation (4) can be used to compute the output impedance by treating all $C_i = C_{fly}$. It can be derived that the output impedance for such a case is proportional to the sum of the squared charge multiplier coefficients ($\sum_k a_k^2$).

Fig. 10 presents a comparison of the output impedance for 2 different VCRs realized using four stages of the proposed IFSC topology. VCR=3/16 achieves better output impedance than VCR=8/15 as the values of $\sum_k a_k^2$ are theoretically related by the ratio $(16/15)^2 = 1.14$. From Fig. 10, this ratio has been found to be around 1.25 which is very close to 1.14,

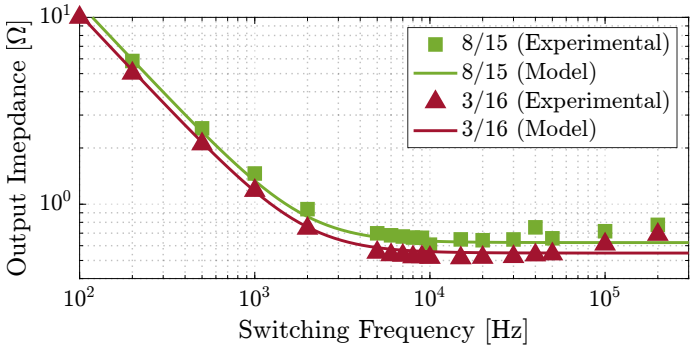


Fig. 10: Variation of output impedance with switching frequency for VCRs realized with the proposed IFSC topology at V_{in}=5 V and I_{out}=200 mA.

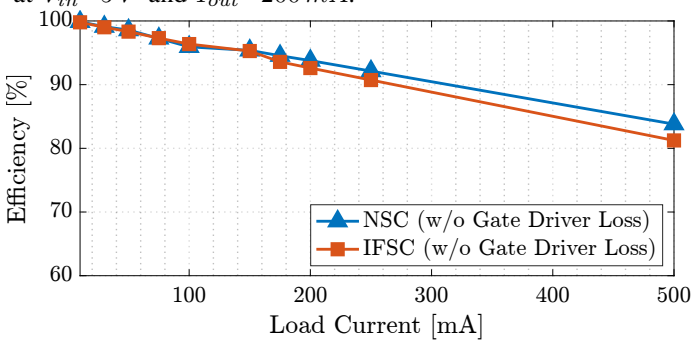


Fig. 11: Load regulation comparison between NSC and IFSC topologies for VCR=14/15 at V_{in}=5 V and f_{sw}=1 kHz.

considering the fact that ESR and parasitic resistances have not been accounted for which can explain the marginal difference.

Figure 11 compares the load regulation of NSC and IFSC topologies for VCR=14/15 at f_{sw}=1 kHz where the converter operates in the *slow-switching limit* (SSL). The only losses in the converter at this operating point are attributed to the charge transfer losses in the capacitors since the conduction loss coming from the *fast-switching limit* (FSL) is insignificant and the gate driver loss has not been incorporated in this measurement. In this implementation, NSC topology has its output impedance 1.06 times lesser than IFSC topology which is why the efficiency for NSC has been observed to be marginally higher for the whole load regulation range from 10 mA to 500 mA.

VI. Conclusion

A novel multi-ratio dc-dc converter topology based on inter-stage feedback has been proposed that can achieve the highest number of ratios possible ($O(4^N)$) with N 2:1 SC stages without requiring any extra stages, thus enabling efficient DVS for wider voltage range. The performance of the proposed DC-DC converter has been compared against recursive (RSC), successive approximation (SAR), and negative-output feedback (NSC) switched-capacitor converters. IFSC topology is a better candidate to minimize the switching losses (bottom-plate parasitic losses and gate driver losses) and capacitor redistribution losses, whereas it is slightly worse than NSC topology for conduction losses. The issues in process integration due to additional voltage rails have been handled in the IFSC topology by limiting all the voltage nodes to swing only between the power supply rails. The proposed IFSC topology can be implemented with a significantly reduced number of reconfiguration switches as compared to NSC topology with the discussed heuristic design strategies. A PCB-based proof of concept prototype was developed to validate the converter performance.

References

[1] D. Jang, J. Kim, U. Lee, J. Suh, and W. Jung, "Techniques for analyzing and reducing voltage conversion ratio transition losses of capacitive dc–dc converters for fast-dvs-enabled systems," *IEEE Transactions on Power Electronics*, vol. 36, no. 10, pp. 10 965–10 969, 2021.

[2] S. Bang, D. Blaauw, and D. Sylvester, "A successive-approximation switched-capacitor dc–dc converter with resolution of $V_{IN}/2^N$ for a wide range of input and output voltages," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 2, pp. 543–556, 2016.

[3] Q. Lu, S. Li, B. Zhao, J. Jiang, Z. Chen, and S. Du, "A dynamically reconfigurable recursive switched-capacitor dc-dc converter with adaptive load ability enhancement," *IEEE Transactions on Power Electronics*, 2023.

[4] S. R. Sanders, E. Alon, H.-P. Le, M. D. Seeman, M. John, and V. W. Ng, "The road to fully integrated dc–dc conversion via the switched-capacitor approach," *IEEE Transactions on Power Electronics*, vol. 28, no. 9, pp. 4146–4155, 2012.

[5] L. G. Salem and P. P. Mercier, "A recursive switched-capacitor dc-dc converter achieving 2^N-1 ratios with high efficiency over a wide output voltage range," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 2773–2787, 2014.

[6] L. Salem and P. Mercier, "An 85%-efficiency fully integrated 15-ratio recursive switched-capacitor dc-dc converter with 0.1-to-2.2 v output voltage range," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*. IEEE, 2014, pp. 88–89.

[7] L. G. Salem, "Recursive switched-capacitor circuit topologies for miniaturized power conversion," Ph.D. dissertation, University of California, San Diego, 2018.

[8] S. Bang, A. Wang, B. Giridhar, D. Blaauw, and D. Sylvester, "A fully integrated successive-approximation switched-capacitor dc-dc converter with 31mv output voltage resolution," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*. IEEE, 2013, pp. 370–371.

[9] S. Bang, "Circuit techniques for power management unit and switched capacitor dc-dc converter." Ph.D. dissertation, University of Michigan, 2016.

[10] W. Jung, D. Sylvester, and D. Blaauw, "12.1 a rational-conversion-ratio switched-capacitor dc-dc converter using negative-output feedback," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*. IEEE, 2016, pp. 218–219.

[11] W. Jung, "Low-power energy efficient circuit techniques for small iot systems," Ph.D. dissertation, University of Michigan, 2017.

[12] H. Kim, C. Park, and C. Kim, "An output-boosted 3-ratio switched-capacitor dc-dc converter with 0.5-to-1.8 v output voltage range for low-power iot applications," in *2022 IEEE 65th International Midwest Symposium on Circuits and Systems (MWSCAS)*. IEEE, 2022, pp. 1–4.

[13] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor dc–dc converters," *IEEE transactions on power electronics*, vol. 23, no. 2, pp. 841–851, 2008.

[14] M. D. Seeman, "A design methodology for switched-capacitor dc-dc converters," California University Berkeley, Dept. of Electrical Engineering and Computer Science, Tech. Rep., 2009.