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Design and Simulation of Non-Inverting and Inverting Mixed Logic 2x4 Decoder Using Mentor Graphics 16nm Technology

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Abstract

Power reduction is one of the major development challenges of this period. In high performance digital frameworks, such as microchips, DSPs, and other applications, low power circuit designs are a requested feature. The primary factors taken into account when comparing any circuit or design are power and speed. When proposing any new design, designers should keep in mind the very impressive but declining chip area. 2x4 Decoder Binary inputs are converted to associated output bits in a pattern using 12 T. A new 2x4 decoder In this work, area optimization with the use of 12T is suggested. The 2:4 decoder is also executed using CMOS logic. The new design and CMOS logic are evaluated in terms of delay and power. Compared to CMOS logic architecture, which typically operates at 0.8V, the new 2x4 decoder design is optimized for power at a rate of 60.72%. PMOS of width (Wp)=64n& length(Ln)=16n,NMOS of width (Wn)=32n & length (Ln)=16n,Fan-out=1, and Wp/Wn=1, after that the designs are assessed at 0.8V with 16nm Mentor Tanner Tool has been used to validate the suggested procedure.

Keywords: Decoder, Low Power Modified Mixed Logic Design, Mentor Graphics, 16nmTechnology .

1 Introduction

Logic gates made with static CMOS circuits make up the majority of the bulk integratedcircuits. The P-MOS pull-up network A CMOS circuit's two primary parts are a CMOS and a N-MOS pull-down network. withstand oscillations in the device and background noise with tenacity. Two benefits of CMOS circuitry are compact transistor sizes and consistent performance at low voltages. Cell-based logic synthesis requires fewer building blocks since CMOS circuits can only receive inputs at the gate terminals of the transistors. In the 1990s, Pass Transistor Logic (PTL) was developed as a rival to CMOS logic. The primary design distinction between pass transistor circuits is determined by which diffusion terminals of the transistors the inputs are connected to (the gate or source/drain). When creating pass transistor circuits, the following two methods are the most widely used. The first method uses the P-MOS and N-MOS transistors separately, whereas the second method combines the two types of transistors in parallel via a transmission gate. Two instances of how developments in VLSI technology have placed additional demands on the design of quick, compact, and low-power logic systems are the need for miniaturization and voltage scaling. When it comes to high-speed computer equipment, such as microprocessors and digital signal processors, designing for power consumption can be difficult. In computers, a decoder is a component that functions as a combinational circuit.

2 Literature Review

Decoder circuits are crucial parts of many digital systems, but because of their large transistor counts, traditional Complementary Metal Oxide Semiconductor (CMOS) implementations consume a lot of power. This has spurred study into alternative design approaches and logic types to lower power consumption in decoder systems without compromising performance.

Over the past 20 years, many strategies have been investigated to deal with this problem. Researchers have already tried with ways to reduce power usage by use transistors rather than CMOS. They looked into possibilities such as TGL, or transmission gate logic. According to Zimmermann and Fichtner (1997), pass transistor logic. These styles had certain advantages, but they also brought about other problems, like poorer driveability. With previous work demonstrating decoders with 50–70% power savings against conventional CMOS, gate diffusion input (GDI) has been a viable low power approach in more recent times (Morgenshtein et al., 2010).

Building on this, in an effort to achieve even greater advancements, scientists have begun fusing several logic styles into hybrid or "modified mixed logic design" (MMLD) architectures. Prior research by Konofaos and Balobas (2017) demonstrated that a dual value logic (DVL) and GDI- enabled MMLD line decoder might provide significant power and latency reductions. Nevertheless, there hasn't been any thorough study or modeling of these hybrid decoder circuits across several process nodes.

By presenting simulation studies of innovative 14 and 15 transistor MMLD decoders implemented with GDI, DVL, and TGL logic on a 130nm process, this study seeks to close that gap. The suggested decoders require almost 50% less transistors than CMOS reference systems. Extensive simulation across the supply voltages demonstrate that for 2-to-4 decoding operations, hybrid MMLD topologies reduce propagation delay and power dissipation. In addition to the immediate advantages, this work offers a performance database and technique to lead the synthesis of MMLD logic in the future.

In conclusion, even though the principles of decoders have long been known, research into developing lower power implementations is still ongoing. This research considerably reduces the delay and power consumption of the decoder by directly building on previous developments in MMLD logic designs. The analytical method based on simulators generates valuable information that assists in the actual fabrication of these designs.

The literature review mentioned above focuses on current methods; using this information, we lowered the number of transistors and suggested a way to lower time delays, power delays, and other characteristics.

3 An Outline of The 2x4 Decoder

Decoder circuit's convert binary data into discrete outputs, which is a crucial function in digital electronics. Their main purpose is to allow the binary input to be used to select one specific output line from a range of options. Decoder's are essential components found in many applications, including microprocessor control unit, a memory systems, and address decoding.

A decoder's fundamental design consists of numerous input lines and numerous output lines. A particular output line is activated by each combination of input values. The decoding capacity is determined by the number of output lines; typical configurations for decoders are 2x4,3x8,and 4x16.Logic gates are used in the implementation of decoder circuits; AND, OR, NAND, or NOR gates are used, depending on the particular design requirements.

A 2x4 decoder is a straightforward yet crucial digital circuit that converts a binary 2-bit input to a 4-bit output. The binary code is represented by the inputs, which are commonly called A and B. The binary input combination determines whether to activate the outputs, which are frequently designated as D3,D2,D1 and D0.The relationship between the inputs and outputs is defined in the matching truth table, which directs the decoder's actions.

A	B	D3	D2	D1	D0
1	1	1	0	0	0
1	0	0	1	0	0
0	1	0	0	1	0
0	0	0	0	0	1

Table 1: Table of Logic for a Non-Inverting 2x4 Decoder.

The Table 1 shows the logic for the 2x4 Non-Inverting decoder. There are four outputs D3,D2,D1 and D0 and it has two inputs they are A and B. Depending on the input values of A and B, one output is High (Logic 1) at a time, and the remaining outputs are Low (Logic 0).

A	B	I3	I2	I1	I0
1	1	0	1	1	1
1	0	1	0	1	1
0	1	1	1	0	1
0	0	1	1	1	0

Table 2: Table of Logic for a Inverting 2 x4 Decoder.

Similarly the Table 2 describes the logic for the 2x4 Inverting decoder. There are four outputs I3,I2,I1 and I0 and it has two inputs A and B. Depending on the input values of A and B, one output is Low (Logic 0) at a time and the remaining outputs are High (Logic 1).The Non-Inverting decoder's

Boolean expressions are D0=A'B', D1=A'B, D2=AB', and D3=AB. In addition, I0=(A'B')', I1=(A'B)', I2=(AB')', and I3=(AB)' are the values for a decoder.

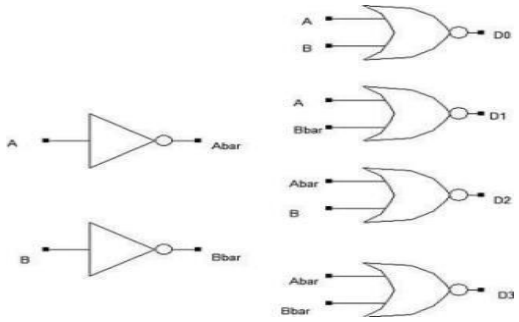

Fig. 1. At the gate level, a 2x4 Non-Inverting decoder is represented.

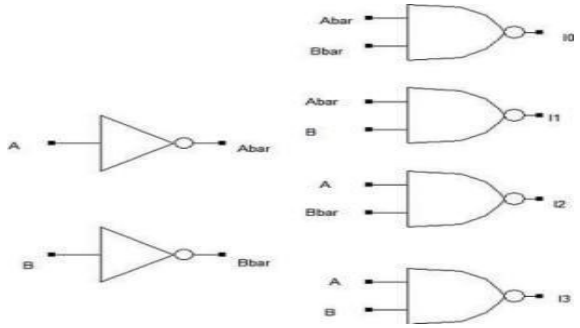

Fig. 2. At the gate level, a 2x4 Inverting decoder is represented.

Four NOR gates and two NOT gates can be used to create a 2x4 Non-Inverter, as shown in Figure 1.

Four NAND gates and two NOT gates can be used to create a 2x4 Inverter, as shown in Figure 2.

4 Modified Mixed Logic for Decoder Implementation

4.1 2x4 Decoder with DVL and TGL Implementation

Transmission gates are used in TGL, a sort of digital logic design, to implement logical functions. Complementary metal-oxide-semiconductor (CMOS) transistors set up to function as bidirectional switches make up transmission gates. When they are turned on, signals can flow through them both ways, essentially sending the input signal to the output.

Fundamental Function:

A 2 by 4 decoder receives two input lines (A and B) and, depending on the combination of inputs, outputs four lines (D0, D1, D2, and D3).

Every output matches a potential combination of inputs. For instance, output D2 will be active if the inputs are A=0 and B=1.

The transistor layouts inside the logic gates will be optimized for both performance and power consumption using the DVL methodology.

The real switching functionality will be implemented using transmission gate logic, which effectively routes signals by taking advantage of the bidirectional characteristics of transmission gates.

Transistors with two distinct threshold voltage levels within the same logic gates are used in the DVL approach.

DVL enhances the logic gates' performance and power consumption characteristics by applying transistors with varying Vth values.

Because TGL and DVL simplify the implementation of NAND and NOR gates, decoders often utilize them. As an example, let's examine the following scenario with two inputs, A and B. By extending the input, we develop a decoder. Lastly, we implement DVL logic architecture with signal A serving as a propagating signal for the outputs D0 and D2.On the other hand, the D1 and D3 outputs of the 2x4 inverting decoder—which has outputs I0 and I2—are constructed using a TGL logic design. On the other hand, outputs I1 and I3 are implemented using the DVL logic design. Both TGL and DVL can be used to make 2x4 decoders inverted, as the diagram illustrates.

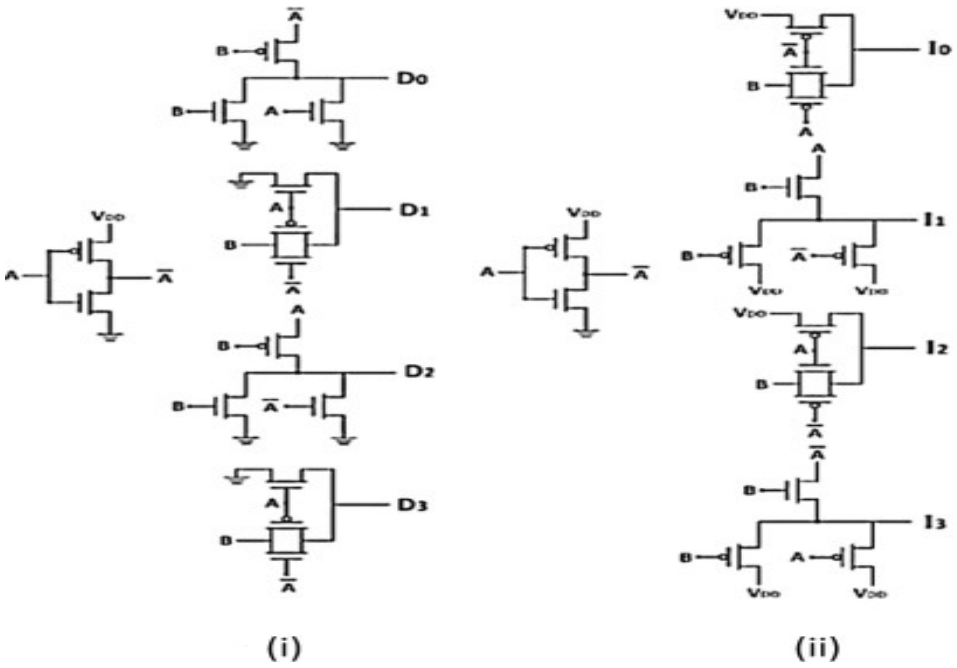

Fig.3. Utilizing DVL and TGL, 2x4 decoders (i). Non- Inverting,(ii).Inverting

Remainder: In order to reduce the quantity of transistors needed for the B to B_bar converter, we represent D0 and D2 using TGL Logic. We concentrate on an inverting input (A_bar) in order to do this.

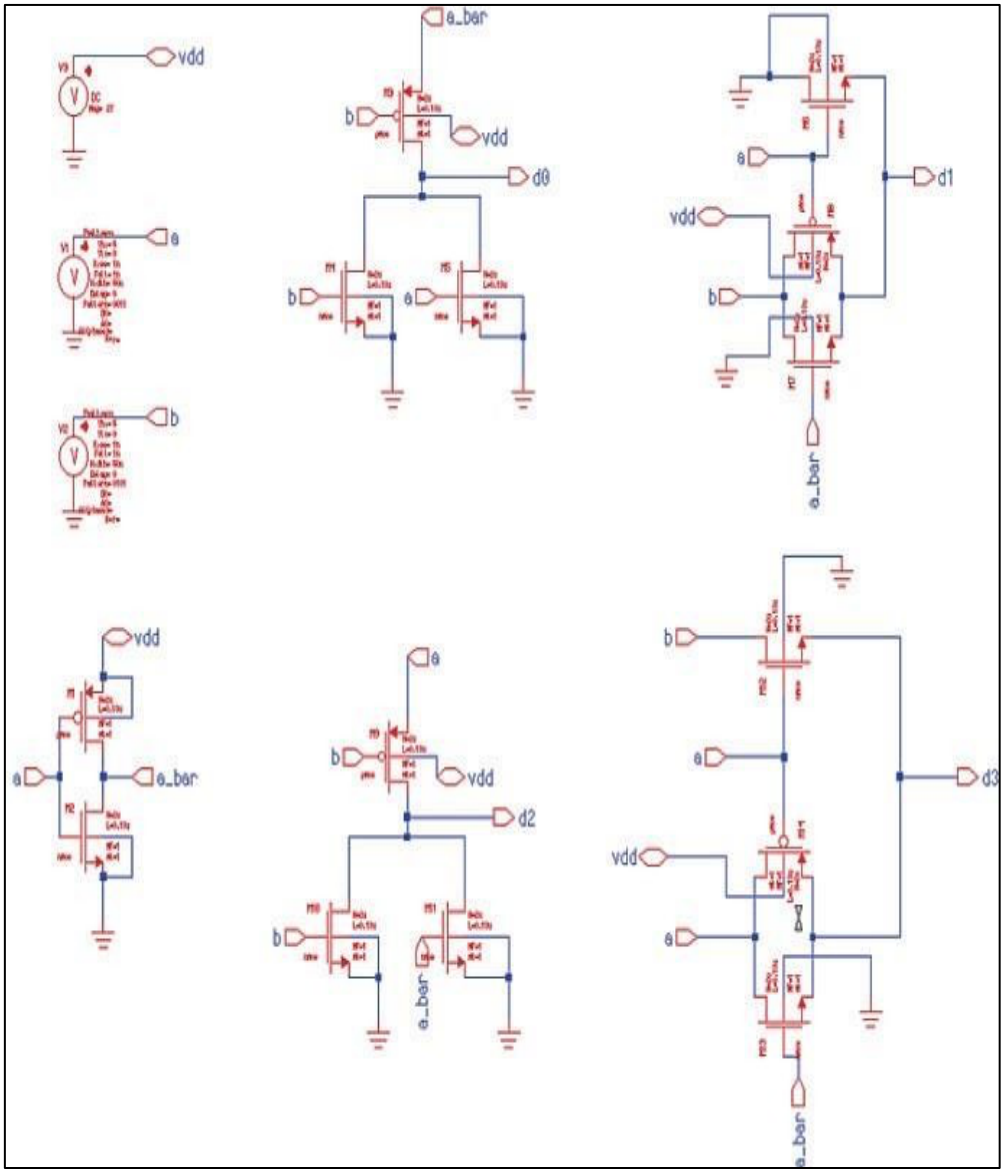

Fig.4. Diagram of TGL and DVL-based Non-Inverting 2x4 decoder.

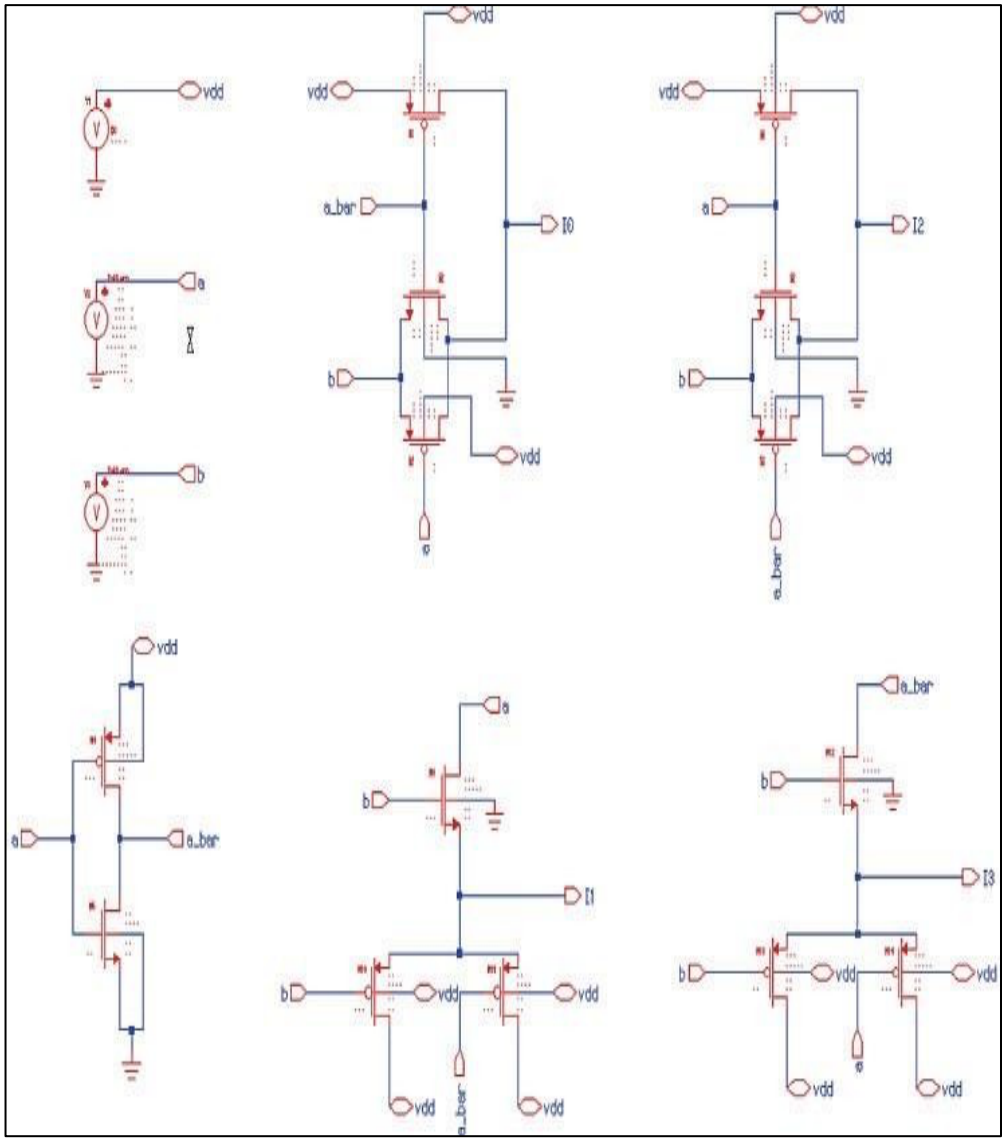

Fig.5. Diagram of TGL and DVL-based Inverting 2x4 decoder.

4.2 Low-Power 2x4 Decoder with 12T Topology

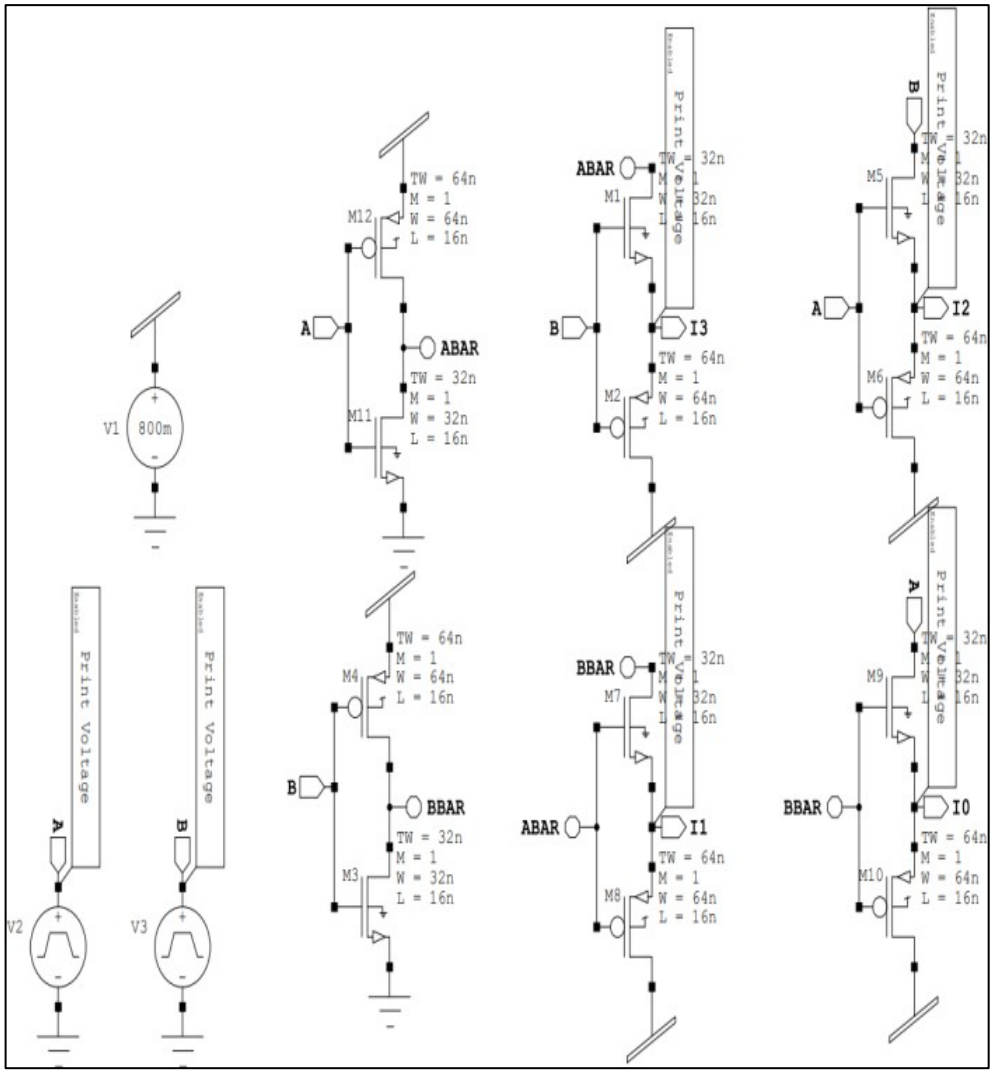

Fig.6. Schematic view of Inverting 2x4 Decoder with 12 Transistors.

The schematic above depicts a 12 transistor 2x4 decoder operating in inversion mode. Two inverters, designated A' and B' in the preceding schematic, will produce the complements of A and B. Two-by-four decoders yield I0, I1, I2, and I3.

Two transistors are needed to make I0, one NMOS in the pull-up area and one PMOS in the pull-down area. When the complement of B and both gates are short, one of the NMOS's inputs is driven by a PMOS source that is connected to VDD, producing the output I0.

Two transistors are needed to make I1, one NMOS in the pull-up area and one PMOS in the pull-down area. When the PMOS source is connected to VDD and one of the NMOS's inputs is driven by B, both of the gates are short combined with the complement of A, producing the output I1.

Two transistors are needed to make I2, one NMOS in the pull-up area and one PMOS in the pull-down area. When the two gates are shorted together with input A and one of the NMOS's inputs is driven with B and the PMOS source is connected to VDD, the result is I2.

Two transistors are needed to make I3, one NMOS in the pull-up area and one PMOS in the pull-down area. When the PMOS source is connected to VDD and one of the NMOS's inputs is powered by A, both gates are shorted together with input B, producing the output I3.

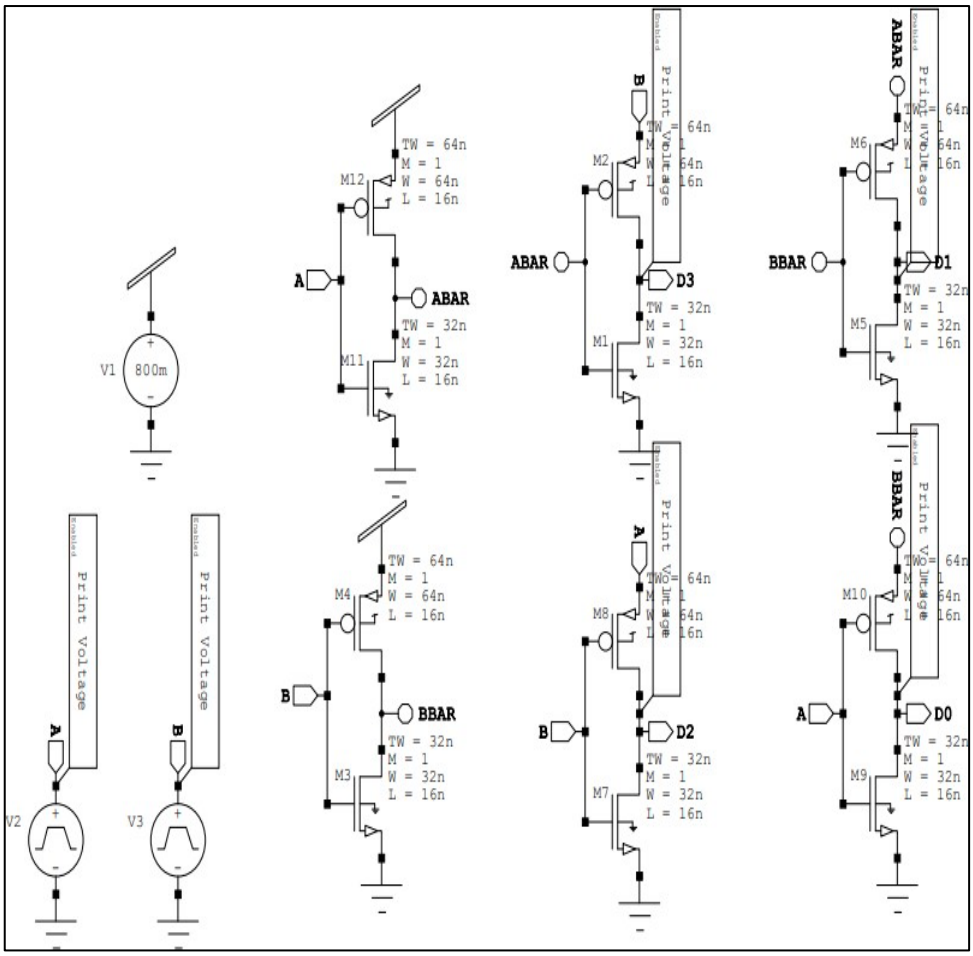

Fig.7. Schematic view of Non- Inverting 2x4 Decoder with 12T

Two transistors are needed to make D0, one PMOS in the pull-up area and one NMOS in the pull- down area. When the NMOS source is connected to VDD and the two gates are shorted together with B, one of the PMOS inputs is driven with the complement of B, producing the output D0.

Two transistors are needed to make D1, one for the pull-up area (PMOS) and one for the pull- down area (NMOS). When the NMOS source is connected to VDD and one of the PMOS inputs is driven by A, both of the gates are short along with the complement of B, producing the output D1.

Two transistors are needed to make D2, one NMOS in the pull-down area and one PMOS in the pull-up area. When the two gates are shorted together with B and one of the PMOS inputs is powered by an NMOS source connected to VDD, the result is D2.

Two transistors are needed to make D3, one PMOS in the pull-up area and one NMOS in the pull-down area. When the NMOS source is connected to the VDD and one of the PMOS inputs is controlled by B, both of the gates are short combined with the complement of A, producing the outputD3.

5 Simulation Results

By using the Mentor Graphics tool, all designs are simulated at 16nm. The width (Wp) and length (Lp) of PMOS and NMOS, respectively, are 1.4 u and 0.35 u for the former and PMOS of width (Wp)=64n& length(Ln)=16n,NMOS of width (Wn)=32n & length (Ln)=16n,Fan-out=1, and Wp/Wn=1, after that the designs are assessed at 0.8V.

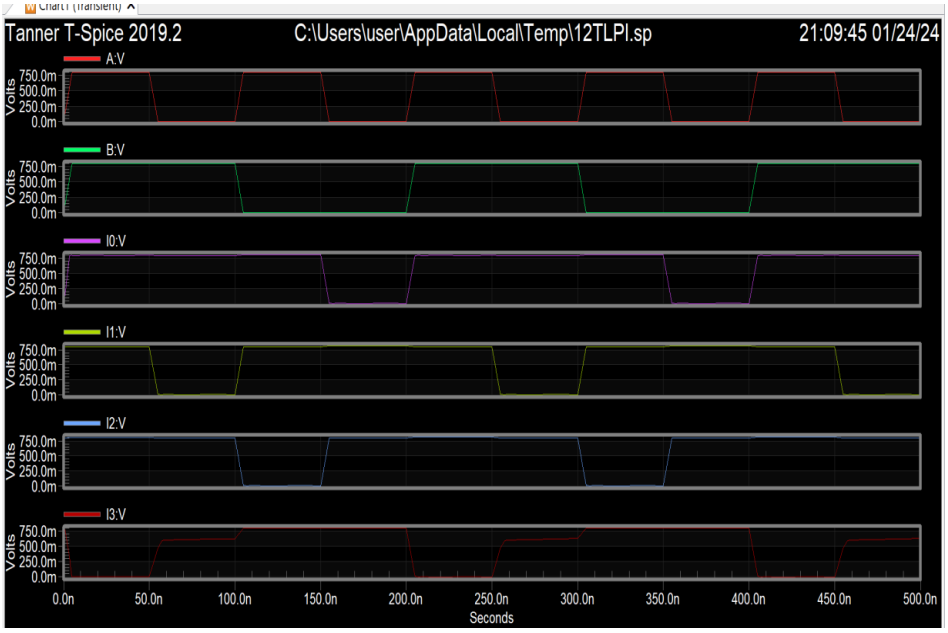

Fig .8. The Low Power Inverting 2x4 Decoder with 12 Transistors Output Waveform

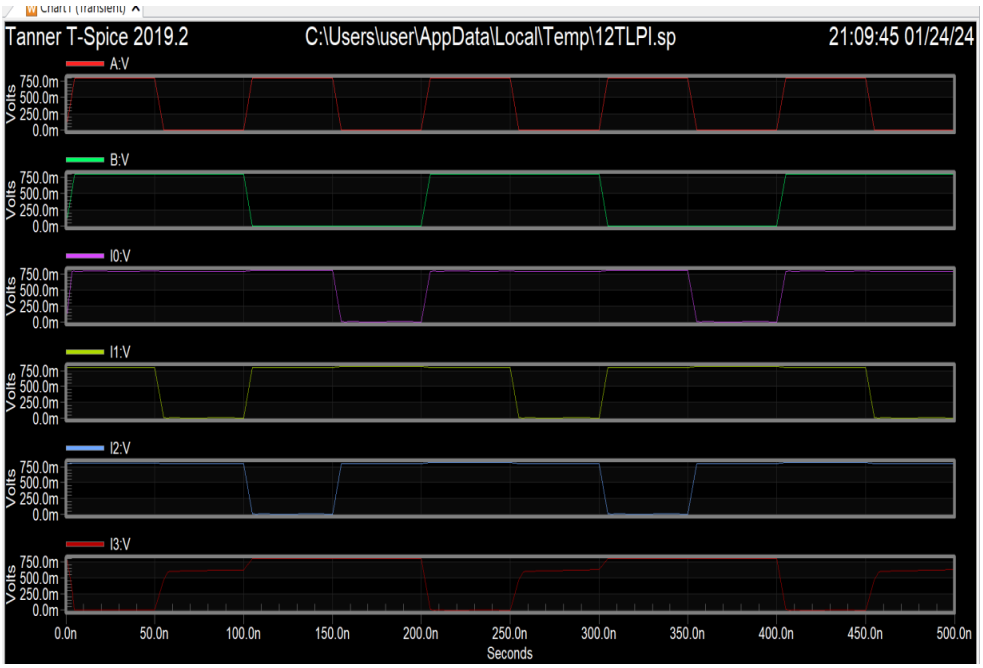

Fig .9. The Low Power Non-Inverting 2x4 Decoder with 12 Transistors Output Waveform.

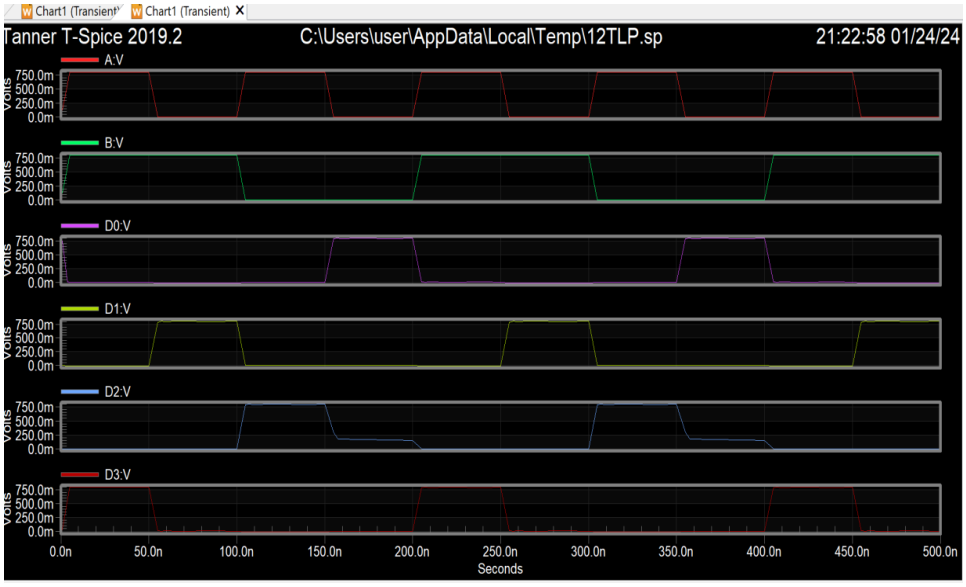

Fig.10. Power Dissipation and Propagation Delay Output Waveform of Non-Inverting 2x4 Decode

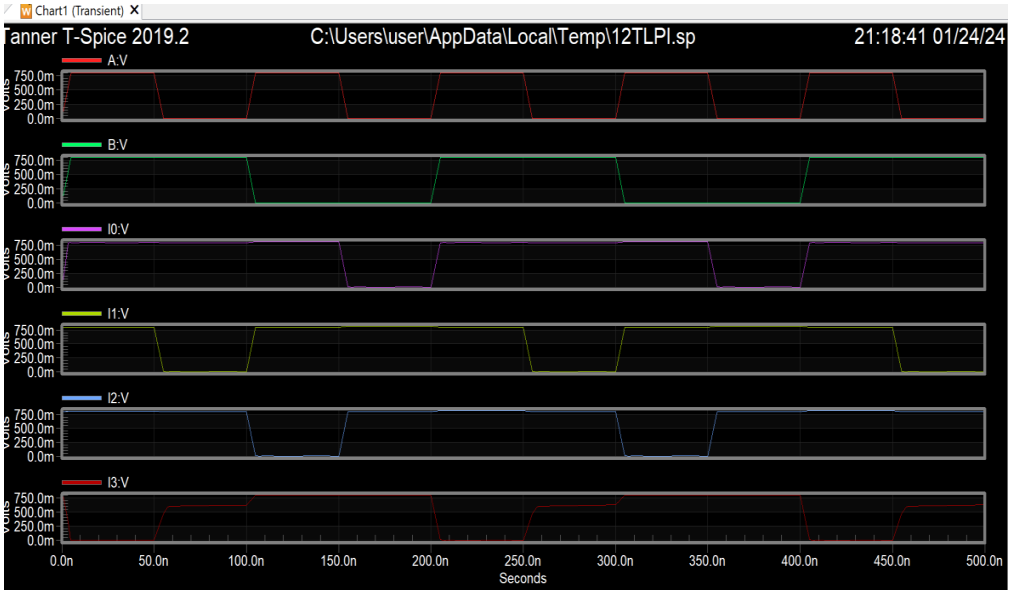

Fig.11. Power Dissipation and Propagation Delay Output Waveform of Inverting 2x4 Decoder.

5.1 Power and Time Delay of 12T Inversion

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Power Results

VV1 from time 0 to 5e-07
Average power consumed -> 2.289190e-07 watts
Max power 9.595293e-06 at time 3.4375e-09
Min power 1.285249e-07 at time 0


Measure information will be written to file "C:\Users\

Measurement result summary
   tdealy          =  100.0569n
```

5.2 Power and Time Delay of 12T Non-Inversion

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Power Results

VV1 from time 0 to 5e-07
Average power consumed -> 1.661826e-07 watts
Max power 7.702886e-06 at time 3.62136e-09
Min power 5.904797e-08 at time 4.5e-07


Measure information will be written to file "C:\User:

Measurement result summary
   tdealy           =    50.0258n
```

6 Comparison Table

S.NO	Method	Avg Power	Static Power	Dynamic Power	Delay
1.	14T LP Decoder	509.8E-9	721P	80.69µ	100.7E-9
2.	14T LPI Decoder	530.8E-9	680.47P	992.41P	211.8E-12
3.	15T HP Decoder	572.5E-9	730.5P	87.143 µ	50.23E-9
4.	15T HPI Decoder	16.81E-6	680.04P	54.15 µ	210.6E-12
5.	12T Decoder PRO	1.129E-6	105.28p	5.36u	631.2E-12
6.	12T Decoder PRO	651.9E-9	1.053n	37.51M	50.34E-9

7 Conclusion

The project using the Mentor Graphics 16nm Technology was validated and finished successfully. In order to create an architecture for decoders, we integrated the CMOS and DVL circuits. Using this method, We Suggest two Topologies for creating decoders With excellent performance and low power consumption.

According to simulation results, our suggested 12T Decoder outperforms. The 2x4 Lpni, Lpi Decoders in terms of power improvement while using less transistors for a delay.

It is therefore appropriate for situations where area and power dissipation are given top priority in the design process, additionally, the Transistors needed for our designed 2x4 decoder take up space on the chip.

The PDP comparison of 2x4 shows that our design is 60.72% more power optimized when comparing power optimization between our design with conventional CMOS Logic at a voltage of 0.8V as opposed to CMOS Logic. The decoder logic's are also shown in the above table; unlike their conventional CMOS equivalents, these logic's can all swing and have less transistors.

7.1 Future Scope

This short describes a technique for creating line decoders that combines static complementary metal oxide semiconductor (CMOS) and transmission gate logic pass transistor dual value logic.

We propose two different topologies for the two four decoders: one with 12 transistors that prioritizes power delay performance, and another with 12 transistors that focuses on decreasing transistor count and power dissipation.

In the future, both inverting decoders could be designed for every scenario. Address creation is a particularly good use case for the suggested decoder.

References

[1] The article "Design of Low Power, High Performance 2-4 and 416 Mixed-Logic Line Decoders" was published in the IEEE Transactions on Circuits and Systems-II Express Briefs, Vol. 64, No. 2, February 2017. It was written by D. Balobas and N. Konofaos.

[2] The article "Design of Area Efficient High-Performance 2-4 and 4-16 Mixed-Logic Line Decoders" was published in December 2017 in the International Journal of Professional Engineering Studies, Volume 9, Issue 4.

[3] The article "Design of Decoders using Mixed Logic for Various Applications" was published in August 2017 in the International Journal of Engineering and Advanced Technology (IJEAT), Volume 6, Issue 6. Simma, Ranjitha, Pasumarthy, and Srikanth.

[4] "Design of Low-Power 2–4 MixedLogic Line Decoders With Clock Based Technique," Ku. Priyanka M. Raut, Dr. R. M. Deshmukh, International Research Journal of Engineering and Technology (IRJET), e-ISSN: 2395-0056, Volume: 05 Issue: 05 | May-2018.

[5] Andrzej Kos, Łukasz Zachara, and Ireneusz Brzozowski INTL JOURNAL OF ELECTRONICS AND TELECOMMUNICATIONS, VOL. 59, NO. 4, PP. 405–413 December 2013, "Designing Method of Compact n-to-2n Decoders." 10.2478/eletel-2013-0050 is the DOI.

[6] Kokkanti Faseeha Tabassum and Sudhir Dakey, "Design of Area and Power Efficient Line Decoders for SRAM", International Journal of Emerging Technologies in Engineering Research (IJETER), Volume 5, Issue 11, November (2017).

[7] Vipul Bhatnagar, Chandani Attri, and Sujata Pandey, "Optimization of row decoder for 128x128 6T SRAMs", International Conference on VLSI Systems, Architecture, Technology and Applications (VLSISATA), £J18_1_4 799-7926-4115/$31.00©2015 IEEE.

[8] Arvind Kumar Mishra, Debiprasad Priyabrata Acharya, and Pradip Kumar Patra "Novel Design Technique of Address Decoder for SRAM", IEEE International Conference on Advanced Communication Control and Computing Technologies (ICACCCT), ISBN No. 978-1-4799-3914-5/14/$31.00 ©20141EEE.

[9] M. Turi and J. Frias, "High-performance low-power selective precharge schemes for address decoder", IEEE Trans. On Circuits & Systems, vol. 55, no. 9, pp. 917-621, Sept. 2008.

[10] D Komali, S. Sridhar, J. Saibabu, B. Rohini Kumar and MD. Ameena, "Design of Low-Power High-Performance 2-4 and 4-16 Mixed Logic Line Decoders", International Journal of Innovative Research in Computer and Communication Engineering, ISSN(Online): 2320-9801, Vol. 6, Issue 2, February 2018.